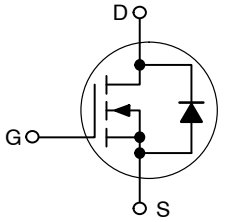
MOSFET – Power, N-Channel, Logic Level, DPAK/IPAK

12 A, 60 V

NTD3055L104, NTDV3055L104

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
60 V	104 mΩ	12 A



N–Channel

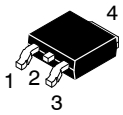
Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

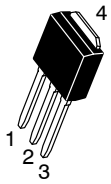
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Tighter V_{SD} Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge
- NTDV and STDV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

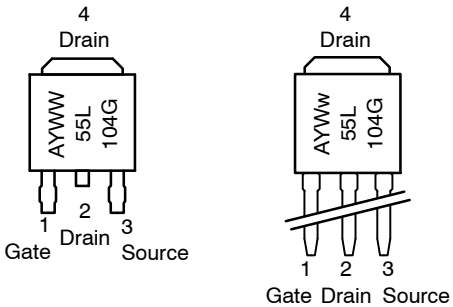


DPAK
CASE 369C
STYLE 2



IPAK
CASE 369D
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENTS



A	= Assembly Location*
55L104	= Device Code
Y	= Year
WW	= Work Week
G	= Pb–Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 10 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage, Continuous – Non–Repetitive ($t_p \leq 10$ ms)	V_{GS} V_{GS}	±15 ±20	Vdc
Drain Current – Continuous @ T_A = 25°C – Continuous @ T_A = 100°C – Single Pulse ($t_p \leq 10$ μs)	I_D I_D I_{DM}	12 10 45	Adc Apk
Total Power Dissipation @ T_A = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (Note 1) Total Power Dissipation @ T_A = 25°C (Note 2)	P_D	48 0.32 2.1 1.5	W W/°C W W
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to +175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, L = 1.0 mH $I_{L(pk)}$ = 11 A, V_{DS} = 60 Vdc)	E_{AS}	61	mJ
Thermal Resistance, – Junction–to–Case – Junction–to–Ambient (Note 1) – Junction–to–Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 71.4 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in^2).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in^2).

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 7.

© Semiconductor Components Industries, LLC, 2016

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 –	 70 62.9	 – –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 – –	 – –	 1.0 10	μAdc
Gate−Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 –	 1.6 4.2	 2.0 –	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 5.0 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	 –	 89	 104	mΩ
Static Drain−to−Source On−Voltage (Note 3) (V_{GS} = 5.0 Vdc, I_D = 12 Adc) (V_{GS} = 5.0 Vdc, I_D = 6.0 Adc, T_J = 150°C)		$V_{DS(on)}$	 – –	 0.98 0.86	 1.50 –	Vdc
Forward Transconductance (Note 3) (V_{DS} = 8.0 Vdc, I_D = 6.0 Adc)		g_{FS}	–	9.1	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	316	440	pF
Output Capacitance		C_{oss}	–	105	150	
Transfer Capacitance		C_{rss}	–	35	70	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{DD} = 30 Vdc, I_D = 12 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω) (Note 3)	$t_{d(on)}$	–	9.2	20	ns
Rise Time		t_r	–	104	210	
Turn−Off Delay Time		$t_{d(off)}$	–	19	40	
Fall Time		t_f	–	40.5	80	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 12 Adc, V_{GS} = 5.0 Vdc) (Note 3)	Q_T	–	7.4	20	nC
		Q_1	–	2.0	–	
		Q_2	–	4.0	–	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 12 Adc, V_{GS} = 0 Vdc) (Note 3) (I_S = 12 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	– –	0.95 0.82	1.2 –	Vdc
Reverse Recovery Time	(I_S = 12 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	–	35	–	ns
		t_a	–	21	–	
		t_b	–	14	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.04	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

Share Feedback
Your Opinion Matters

TYPICAL CHARACTERISTICS

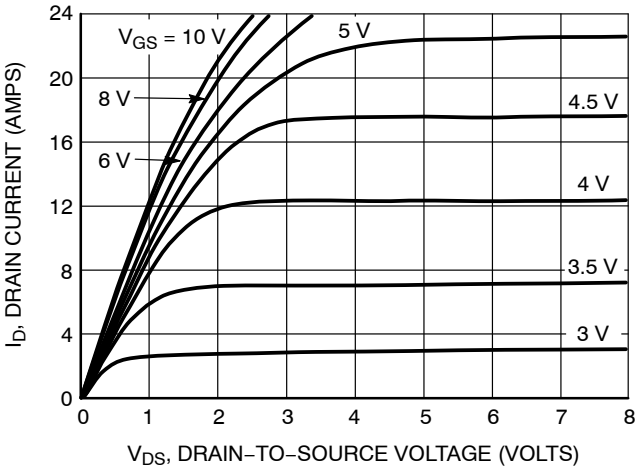


Figure 1. On−Region Characteristics

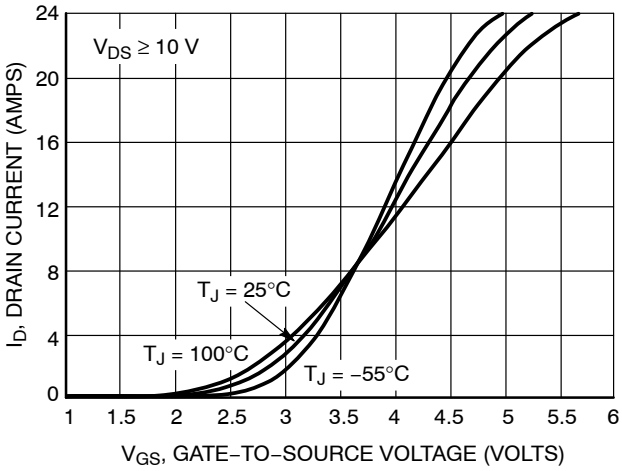


Figure 2. Transfer Characteristics

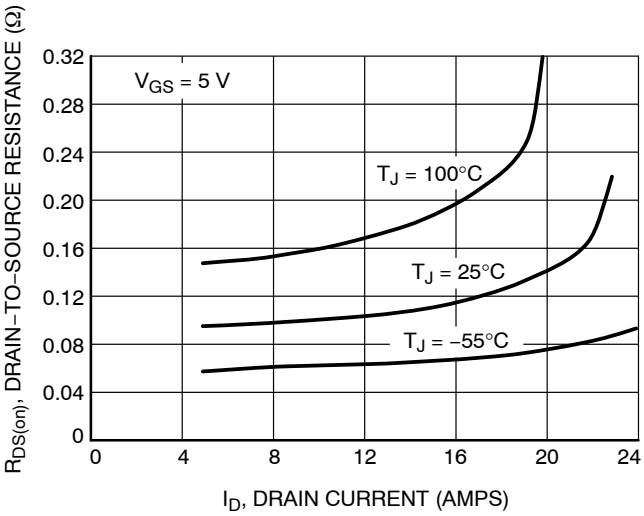


Figure 3. On−Resistance versus Gate−to−Source Voltage

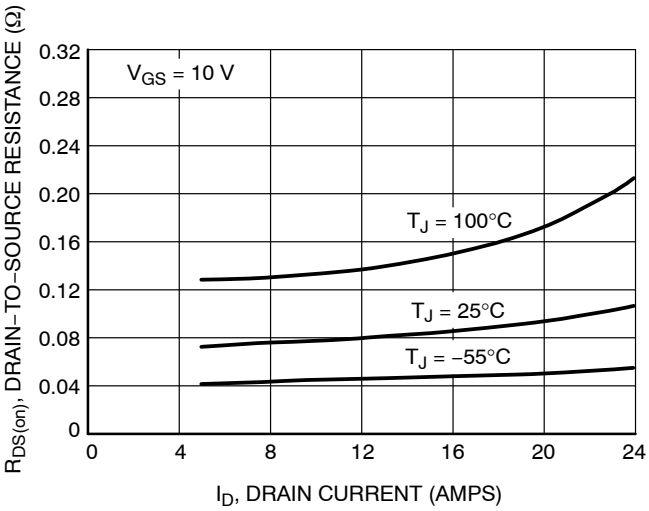


Figure 4. On−Resistance versus Drain Current and Gate Voltage

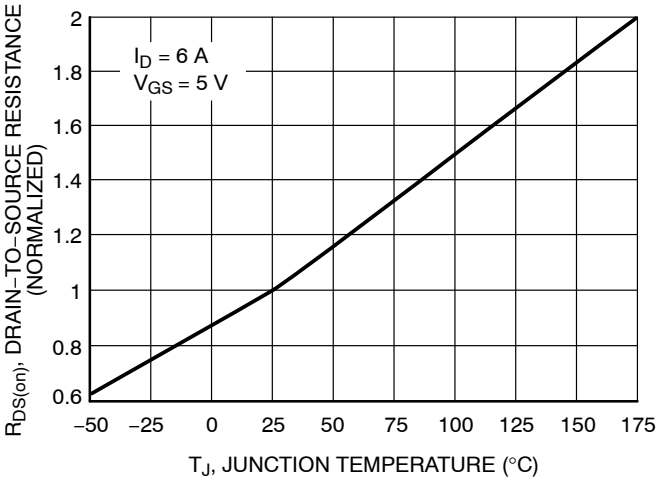


Figure 5. On−Resistance Variation with Temperature

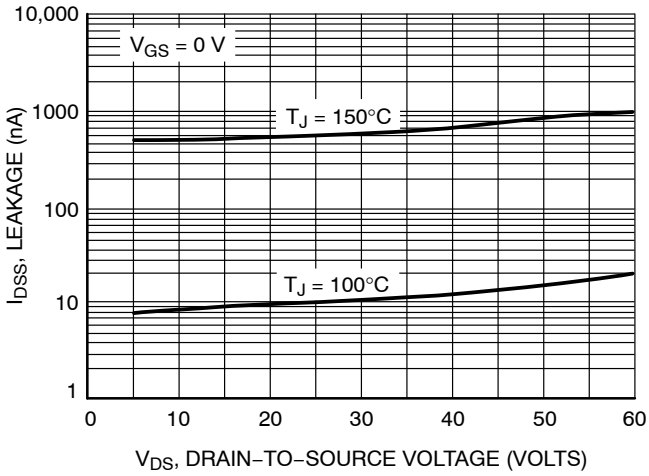


Figure 6. Drain−to−Source Leakage Current versus Voltage

Share Feedback
Your Opinion Matters

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

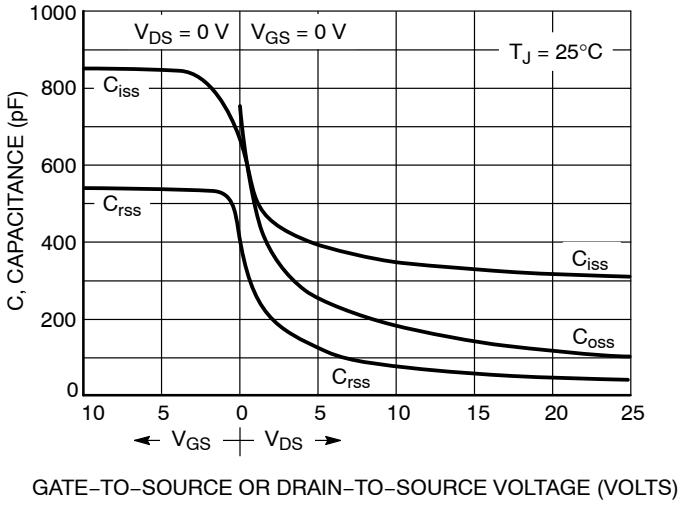


Figure 7. Capacitance Variation

Share Feedback
Your Opinion Matters

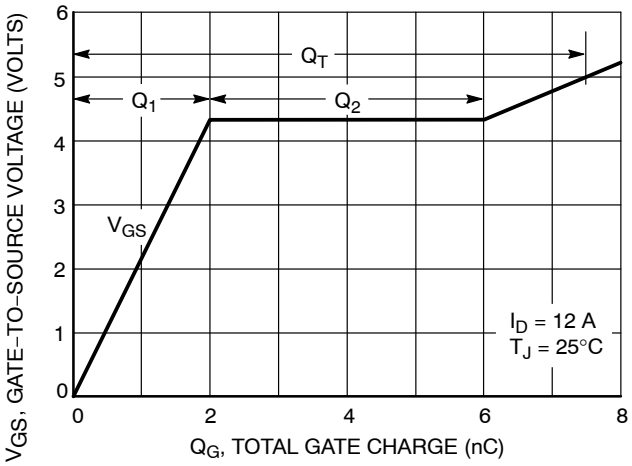


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

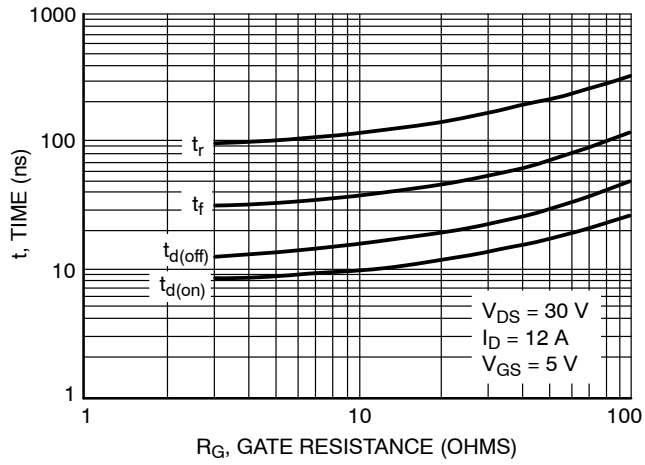


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN−TO−SOURCE DIODE CHARACTERISTICS

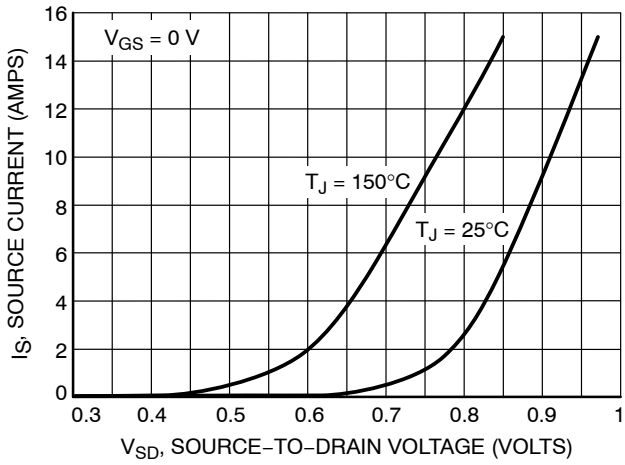


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance − General Data and Its Use.”

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E−FETs can withstand the stress of drain−to−source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

Share Feedback
Your Opinion Matters

SAFE OPERATING AREA

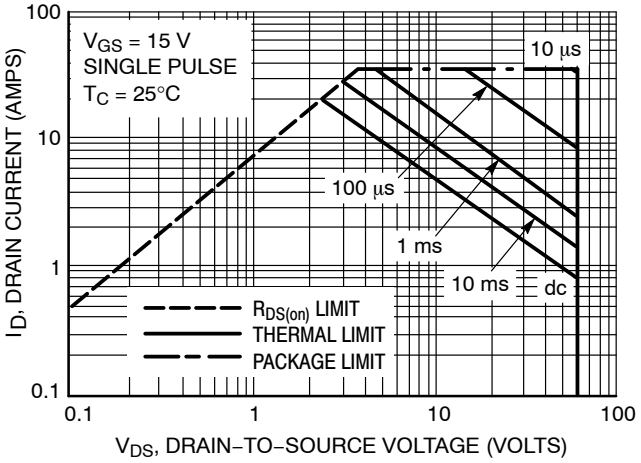


Figure 11. Maximum Rated Forward Biased Safe Operating Area

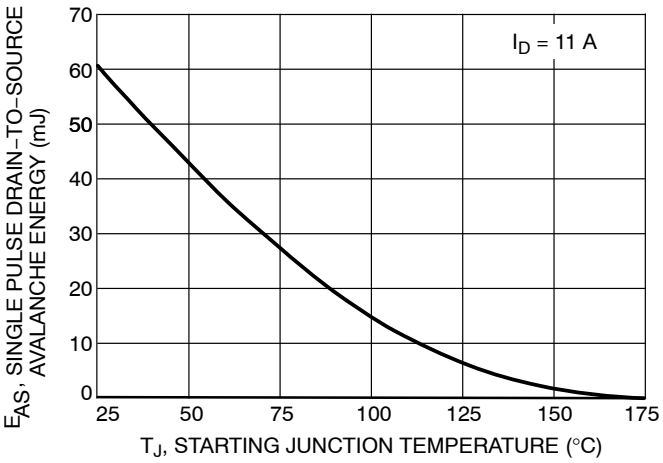


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

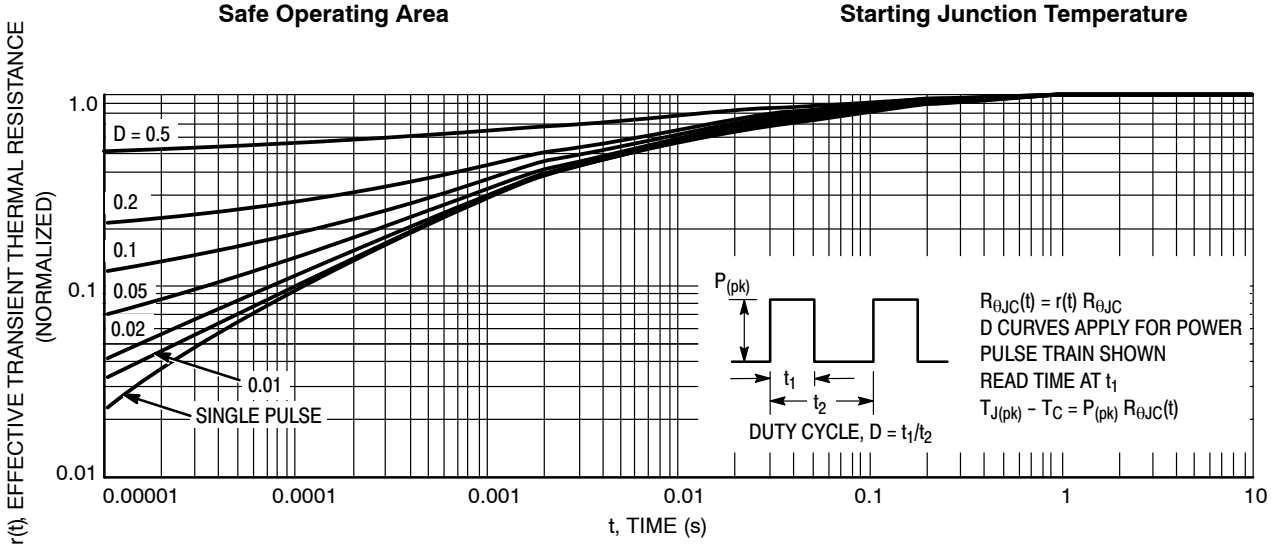


Figure 13. Thermal Response

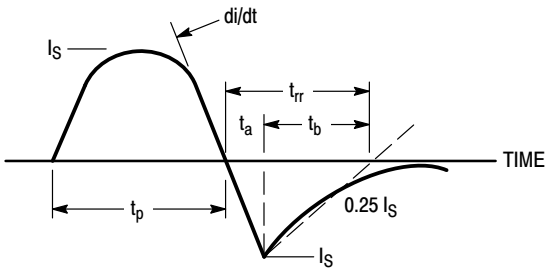


Figure 14. Diode Reverse Recovery Waveform

Share Feedback
Your Opinion Matters

ORDERING INFORMATION

Device	Package	Shipping†
NTD3055L104T4G	DPAK (Pb−Free)	2500 / Tape & Reel
STDV3055L104T4G*	DPAK (Pb−Free)	2500 / Tape & Reel

DISCONTINUED (Note 5)

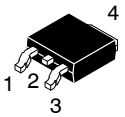
NTD3055L104G	DPAK (Pb−Free)	75 Units / Rail
NTD3055L104−1G	IPAK (Pb−Free)	75 Units / Rail
NTDV3055L104−1G	IPAK (Pb−Free)	75 Units / Rail
NTDV3055L104T4G*	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NTDV and STDV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

5. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

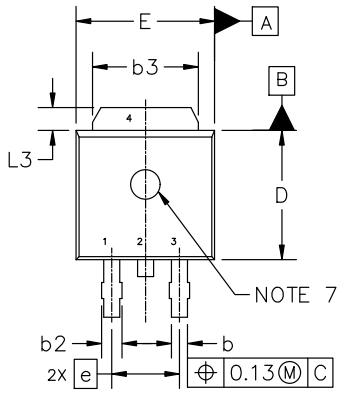
Share Feedback
Your Opinion Matters



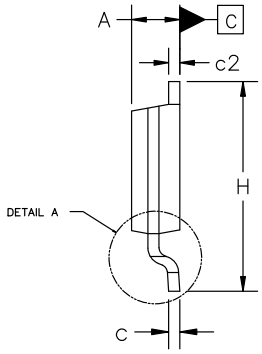
SCALE 1:1

DPAK–3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 14 MAY 2026

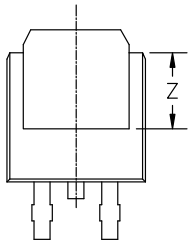


TOP VIEW

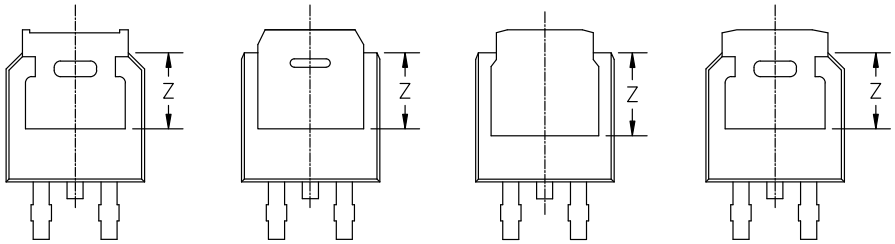


SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



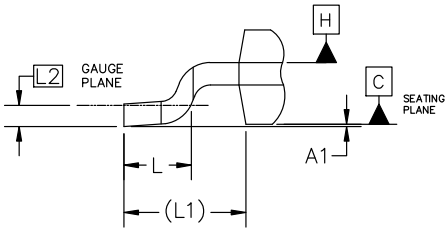
BOTTOM VIEW



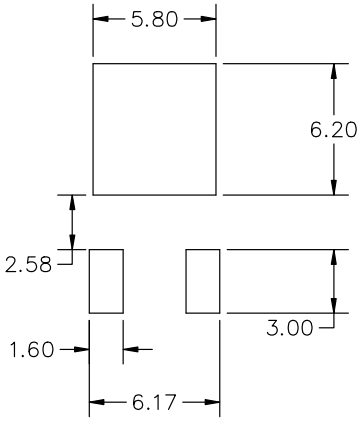
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

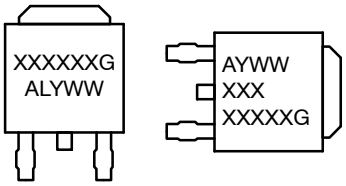
DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK–3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 13 MAY 2026

GENERIC
MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2011

onsemi, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales