Multi-Output Regulator with Buck or Buck-Boost Pre-Regulator, 4× LDO Outputs, Watchdog, 4× Gate Drivers, and SPI

FEATURES AND BENEFITS

- ASIL Compliant: ASIL D safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual
- Automotive AEC-Q100 qualified
- Wide input voltage range, 3.8 to 36 V_{IN} operating range, 40 V_{IN} maximum
- 2.2 MHz buck or buck/boost pre-regulator (VREG: 5.35 V) with low EMI frequency dithering
- Frequency dithering and controlled slew rate help reduce EMI/EMC
- Four internal linear regulators with foldback short-circuit protection
  - VUC: selectable output (3.3 V / 5.0 V) regulator for microcontroller
  - V5A: 5 V general purpose LDO regulator
  - V5P1 and V5P2: two LDO regulators with short-to-battery protection for remote sensors
- OV and UV protection for all output rails provides ability to monitor health of outputs
- Pulse Width Watchdog (PWWD), Window Watchdog (WWD), and Q&A Watchdog (QAWD)
- Floating gate drivers (with charge pumps) for external switched load control
- Analog multiplexor (AMUX) reports operational values of multiple important parameters
- Safety signal (POE) can disable a separate function (e.g., motor driver) due to a Watchdog Failure

Continued on next page...

APPLICATIONS

Provides system power (for microcontroller/DSP, CAN, sensors, etc.) and high-side gate driver control (for motor phases and other switched loads such as solenoid valves and SS relays) in:

- Industrial applications
- Electronic power steering (EPS)
- Advanced braking systems (ABS)
- Transmission control units (TCU)
- Emissions control modules
- Other automotive applications

DESCRIPTION

The A81407 is ideal for both automotive and industrial applications, where high temperature operation, a high level of integration, and robust solutions are required.

The IC integrates a buck or buck/boost pre-regulator, four LDOs, and four floating gate drivers. The pre-regulator uses a buck or buck/boost topology to efficiently convert input voltages into a tightly regulated intermediate voltage. Frequency dithering and slew control help reduce EMI. The output of the pre-regulator supplies a 3.3 V / 375 mA linear regulator, a 5 V / 150 mA linear regulator, and two 5 V / 120 mA linear regulators. All of the outputs are protected against short circuits, and two are further protected from short-to-supply voltage in case they are used remotely.

The independent floating gate drivers can be used for input supply disconnect or reverse-supply protection. They can also be used for switched loads such as motor phases, solid state relays, and solenoid valves. They have the capability of controlling N-channel MOSFETs through SPI. An integrated charge pump allows the driver outputs to maintain the power MOSFETs in the on-state over the full supply range with high phase-voltage slew rates.

Diagnostic outputs from the A81407 include a Watchdog Fault (WD_Fn), power-on reset (NPOR), and a fault flag (FFn) to alert the microprocessor that a fault has occurred. The microprocessor can read fault registers through SPI and operational status via an analog multiplexor.

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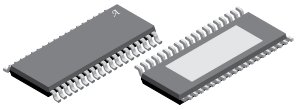
PACKAGE

38-Pin eTSSOP (suffix LV)



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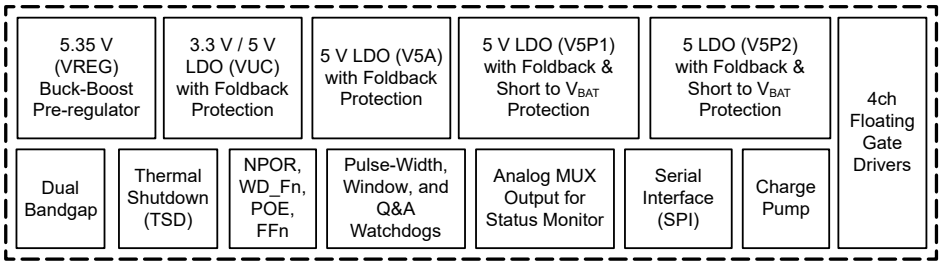
ISO 26262 ASIL Compliant



A81407 Simplified Block Diagram

FEATURES AND BENEFITS (continued)

- Pin-to-pin and pin-to-ground tolerant at every pin
- Control and diagnostic reporting through secure SPI
  - □ 16-bit Data Transfers
  - □ 5-bit Message ID
  - □ 5-bit CRC
  - □ Read-Back Register
  - □ 3-bit Frame Counter
  - □ Chip ID
- Logic enable input (ENB) for microprocessor control
- High-voltage ignition enable input (ENBAT)
- Thermal shutdown protection
- –40°C to 150°C junction temperature range

DESCRIPTION (continued)

Dual bandgaps, one for regulation and one for fault checking, improve safety coverage and fault detection of the A81407.

The A81407 contains three types of watchdog timers: Pulse Width Watchdog (PWWD), Window Watchdog (WWD), and Q & A Watchdog (QAWD). The watchdog timers can be put into various operating states via secure SPI commands.

The A81407 is supplied in a 38-lead eTSSOP package (suffix "LV") with exposed power pad.

SELECTION GUIDE

Part Number	V_{UC} (V)	Package	Packing [1]	Lead Frame
A81407KLVATR	3.3	38-pin eTSSOP with thermal pad	4000 pieces per 7-inch reel	100% matte tin
A81407KLVATR-1	5			

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{VIN}		−0.3 to 40	V
ENBAT	V_{ENBAT}		−0.3 to 40	V
	I_{ENBAT}		±75	mA
LX	V_{LX}		−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
		t < 50 ns	V_{VIN} + 3	V
GU, GV, GW, GVBB	V_{GU}, V_{GV}, V_{GW}, V_{GVBB}		V_{Sz} – 0.3 to V_{Sz} + 12	V
SU, SV, SW, SVBB	V_{SU}, V_{SV}, V_{SW}, V_{SVBB}		–6 to V_{VIN} + 5	V
VCP (Gate Drivers)	V_{VCP}		V_{VIN} – 0.3 to V_{VIN} + 12	V
CP1 (Gate Drivers)	V_{CP1}		V_{VIN} – 0.3 to V_{VIN} + 8	V
CP2 (Gate Drivers)	V_{CP2}		V_{VIN} – 0.3 to V_{VIN} + 12	V
VCP2 (Pre-Regulator)	V_{VCP2}		V_{VIN} – 0.3 to V_{VIN} + 8	V
CP2C1 (Pre-Regulator)	V_{CP2C1}		−0.3 to V_{VIN} + 0.3	V
CP2C2 (Pre-Regulator)	V_{CP2C2}		V_{VIN} – 0.3 to V_{VIN} + 8	
V5P1, V5P2	V_{V5P1}, V_{V5P2}	Independent of V_{VIN}	−1.0 to 40	V
All other pins			−0.3 to 7	V
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	eTSSOP-38 (LV) package	30	°C/W

[3] Additional thermal information available on the Allegro website.

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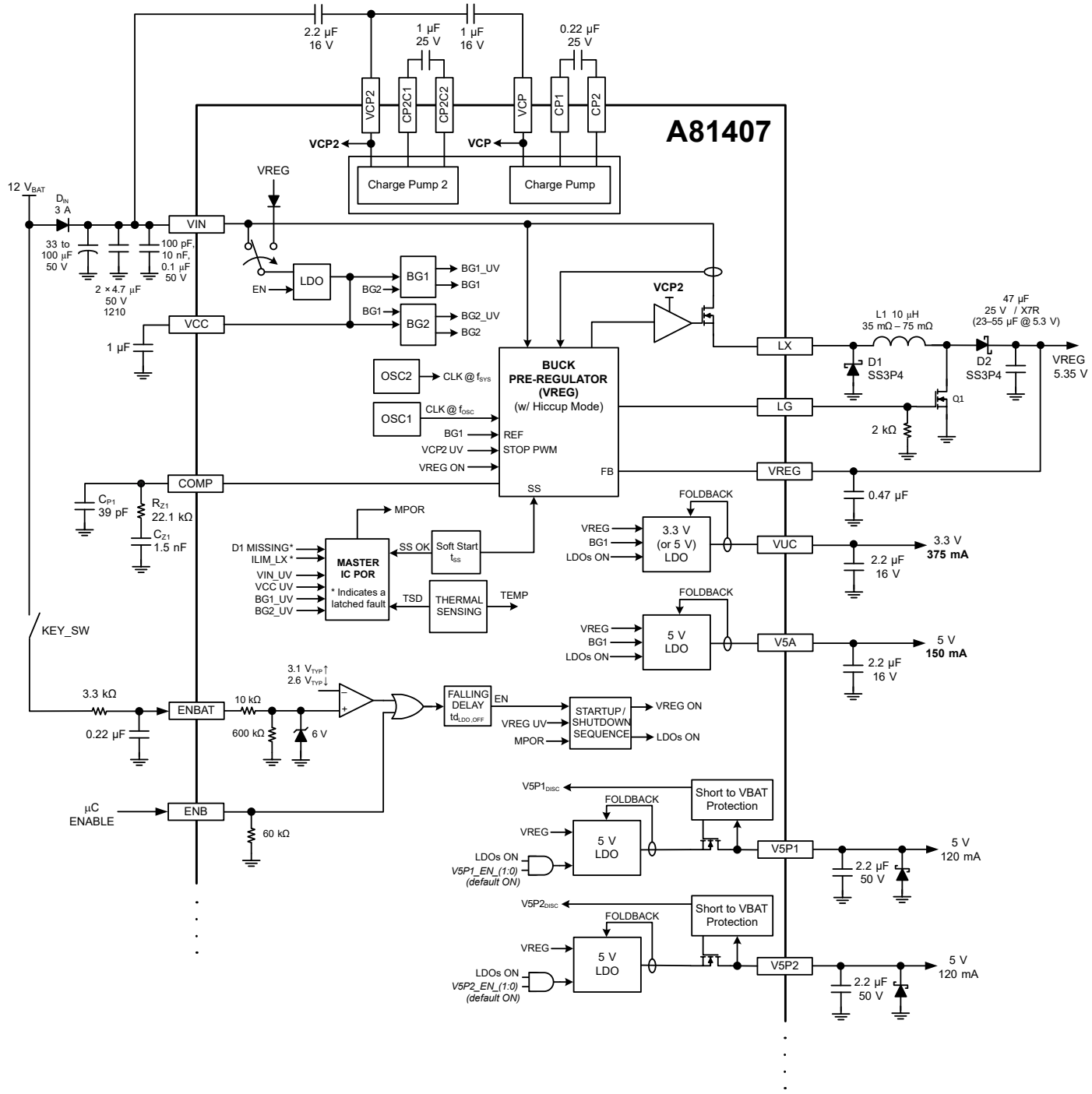
FUNCTIONAL BLOCK DIAGRAM



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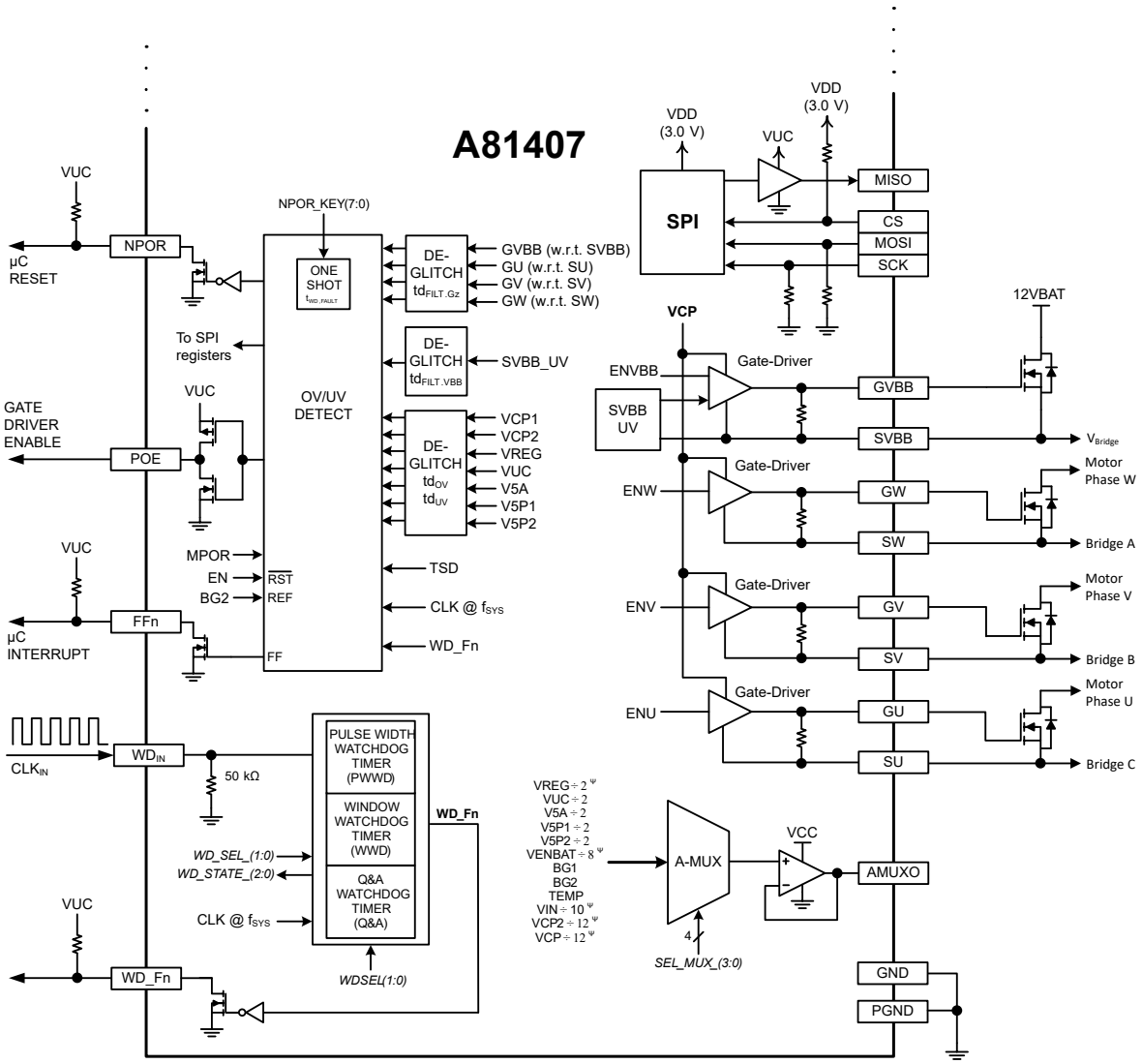
FUNCTIONAL BLOCK DIAGRAM (continued)



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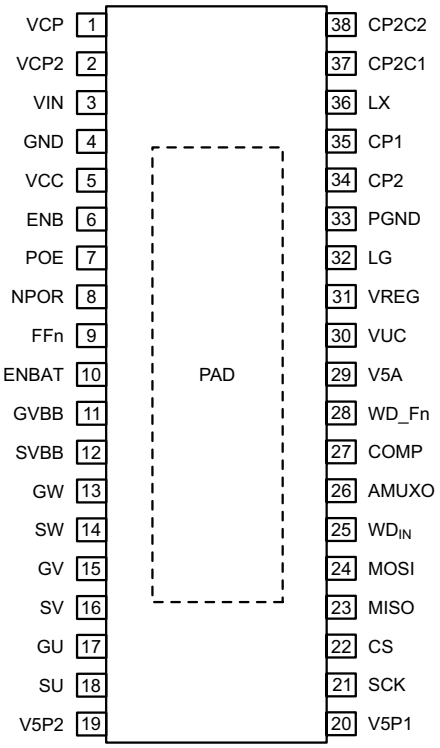

Package LV, 38-Pin eTSSOP Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCP	Charge pump reservoir capacitor connection, for phase disconnects
2	VCP2	Charge pump reservoir capacitor connection, for buck/boost regulator
3	VIN	Input voltage pin
4	GND	Ground
5	VCC	Internal voltage regulator bypass capacitor pin
6	ENB	Logic enable input from a microcontroller or DSP
7	POE	Gate drive enable, latches low to put the system into a safe state
8	NPOR	Active-low, open-drain VUC fault detection output. Using SPI programming, Watchdog (WD) fault and/or V5A can be added to the NPOR logic.
9	FFn	Fault Flag to the microcontroller, open-drain, active low
10	ENBAT	Ignition enable input from the key/switch via a series resistor
11	GVBB	Battery line MOSFET gate drive
12	SVBB	Battery line MOSFET source reference
13	GW	W phase MOSFET gate drive
14	SW	W phase MOSFET source reference
15	GV	V phase MOSFET gate drive
16	SV	V phase MOSFET source reference
17	GU	U phase MOSFET gate drive
18	SU	U phase MOSFET source reference
19	V5P2	5 V protected regulator output
20	V5P1	5 V protected regulator output
21	SCK	SPI clock input from the microcontroller
22	CS	SPI Chip Select input from the microcontroller
23	MISO	SPI data output to the microcontroller (Master Input, Slave Output)
24	MOSI	SPI data input from the microcontroller (Master Output, Slave Input)
25	WDIN	Watchdog refresh input from a microcontroller or DSP
26	AMUXO	Analog Multiplexer output
27	COMP	Error amplifier compensation network pin for the buck/boost pre-regulator
28	WD_Fn	Open-drain, WD fault output. Latches low if a WD fault is detected.
29	V5A	5 V regulator output
30	VUC	3.3 V regulator output (or 5V for A81407-1)
31	VREG	Voltage feedback input of the pre-regulator and input to the LDOs
32	LG	Boost gate drive output for the buck/boost pre-regulator
33	PGND	Power ground
34	CP2	Charge pump capacitor connection
35	CP1	Charge pump capacitor connection
36	LX	Switching node for the buck/boost pre-regulator
37	CP2C1	Charge pump capacitor connection
38	CP2C2	Charge pump capacitor connection
–	PAD	Exposed thermal pad

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ELECTRICAL CHARACTERISTICS [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage [2]	V_{VIN}	After V_{VIN} > $V_{VIN(START)}$ and VREG in regulating, Buck-Boost Mode	3.8	13.5	36	V
		After V_{VIN} > $V_{VIN(START)}$ and VREG in regulating, Buck Mode	5.5	13.5	36	V
VIN UVLO Start Voltage	$V_{VIN(START)}$	V_{VIN} rising	4.55	4.8	5.05	V
VIN UVLO Stop Voltage	$V_{VIN(STOP)}$	V_{VIN} falling	3.25	3.5	3.75	V
VIN UVLO Hysteresis	$V_{VIN(HYS)}$	$V_{VIN(START)}$ – $V_{VIN(STOP)}$	–	1.3	–	V
VIN Supply Quiescent Current [1][3]	I_Q	V_{VIN} = 13.5 V, V_{VREG} = 5.6 V (no PWM)	–	13	–	mA
	$I_{Q(SLEEP)}$	V_{VIN} = 13.5 V, V_{ENBAT} = Low and V_{ENB} = Low, T_J = 25°C	–	–	13	µA
PWM SWITCHING FREQUENCY AND DITHERING						
Switching Frequency	f_{OSC}	Dithering off	2.0	2.2	2.4	MHz
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±10	–	%
VIN Dithering Start Threshold [2]	$V_{VIN(DITHER,ON)}$	V_{VIN} rising	8.5	9.0	9.5	V
		V_{VIN} falling	–	17	–	V
VIN Dithering Stop Threshold [2]	$V_{VIN(DITHER,OFF)}$	V_{VIN} falling	7.8	8.3	8.8	V
		V_{VIN} rising	–	18	–	V
SYSTEM (WATCHDOG) CLOCK						
Internal Clock Frequency	f_{SYS}		–	8	–	MHz
Internal Clock Tolerance	$f_{SYS(TOL)}$		–5	–	+5	%
CHARGE PUMP (VCP AND VCP2)						
VCP2 Output Voltage (for Pre-Regulator)	V_{VCP2}	V_{VCP2} – V_{VIN}, V_{VIN} ≥ 9 V, I_{VCP2} > –5 mA, Buck Mode	4.1	6.6	–	V
		V_{VCP2} – V_{VIN}, 5.5 V < V_{VIN} ≤ 9 V, I_{VCP2} > –5 mA, Buck Mode	3.6	4.4	–	V
		V_{VCP2} – V_{VIN}, 3.8 V < V_{VIN} ≤ 5.5 V, V_{REG} = 5.35 V, I_{VCP2} > –5 mA, Buck-Boost Mode	3.0	3.8	–	V
VCP Output Voltage (for Gate Drivers)	V_{VCP}	V_{VCP} – V_{VIN}, V_{VIN} > 9 V, I_{VCP} > –1 mA, Buck Mode	9	10	–	V
		V_{VCP} – V_{VIN}, 5.5 V < V_{VIN} ≤ 9 V, I_{VCP} > –1 mA, Buck Mode	8	10	–	V
		V_{VCP} – V_{VIN}, 3.8 V < V_{VIN} ≤ 5.5 V, V_{VREG} = 5.35 V, I_{VCP} > –1 mA, Buck-Boost Mode	6.6	9.5	–	V
Switching Frequency	f_{CPx}		–	65	–	kHz
VCC PIN VOLTAGE						
Output Voltage	V_{VCC}	V_{VREG} = 5.35 V	–	4.4	–	V
THERMAL PROTECTION						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	165	–	–	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{VCP(UV,H)}$ and V_{VREG} in regulating are satisfied before V_{VIN} is reduced.

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE SPECIFICATIONS						
Pre-Regulator Output Voltage [2]	V_{VREG}	V_{VIN} = 13.5 V, 0.1 A < I_{VREG} < 1.2 A	5.25	5.35	5.45	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWM(OFFS)}$	V_{COMP} for 0% duty cycle	–	480	–	mV
LX Rising Slew Rate [2]	SR_{LXRISE}	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A	–	1.4	–	V/ns
LX Falling Slew Rate [2]	SR_{LXFALL}	V_{VIN} = 13.5 V, 90% to 10%, I_{VREG} = 1 A	–	1.5	–	V/ns
Buck Minimum On-Time	$t_{ON(BUCK,MIN)}$		–	85	160	ns
Buck Maximum Duty Cycle	$D_{BUCK(MAX)}$	V_{VIN} < 7.8 V	–	–	100	%
Boost Duty Cycle	D_{BST}	After V_{VIN} > $V_{VIN(START)}$, VREG regulating, V_{VIN} = 3.8 V	–	60	–	%
		V_{VIN} = 6.5 V	–	29	–	%
COMP to LX Current Gain	gm_{POWER}		–	4.57	–	A/V
Slope Compensation [2]	S_E		1.1	1.62	2.15	A/µs
INTERNAL MOSFET						
MOSFET On Resistance	$R_{DS(on)}$	V_{VIN} = 13.5 V, T_J = –40°C [2], I_{DS} = 0.1 A	–	60	90	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [3], I_{DS} = 0.1 A	–	95	115	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	160	190	mΩ
MOSFET Leakage Current	$I_{FET(LKG)}$	V_{ENBAT} ≤ 2.2 V, V_{ENB} = Low, V_{LX} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 85°C [3]	–	–	10	µA
		V_{ENBAT} ≤ 2.2 V, V_{ENB} ≤ Low, V_{LX} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 150°C	–	50	150	µA
ERROR AMPLIFIER						
Open Loop Voltage Gain	A_{VOL}		–	60	–	dB
Transconductance	gm_{EA}	V_{SS} (internal signal) = 750 mV	520	720	920	µA/V
		V_{SS} (internal signal) = 500 mV	260	360	460	µA/V
Output Current	$I_{O(EA)}$		–	±75	–	µA
Maximum Output Voltage	$V_{O(EA,MAX)}$	V_{VIN} < 8.5 V	1.2	1.52	2.1	V
		V_{VIN} > 9.5 V	0.9	1.22	1.7	V
Minimum Output Voltage	$V_{O(EA,MIN)}$		–	–	300	mV
COMP Pull-Down Resistance	R_{COMP}	HICCUP = 1 or FAULT = 1 or V_{ENBAT} = Low and V_{ENB} = Low	–	1	–	kΩ

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BOOST MOSFET (LG) GATE DRIVER						
LG High Output Voltage	$V_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V	4.6	–	5.35	V
LG Low Output Voltage	$V_{LG(OFF)}$	V_{VIN} = 13.5 V, V_{VREG} = 5.35 V	–	0.2	0.4	V
LG Source Current [1]	$I_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	−300	–	mA
LG Sink Current [1]	$I_{LG(OFF)}$	V_{VIN} =13.5 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	150	–	mA
SOFT-START						
SS Ramp Time [2]	t_{SS}		–	900	–	µs
SS PWM Frequency Foldback	$f_{SW(SS)}$	0 V ≤ V_{VREG} < 0.67 V typical	–	f_{OSC}/8	–	–
		0.67 V ≤ V_{VREG} < 1.34 V typical	–	f_{OSC}/4	–	–
		1.34 V ≤ V_{VREG} < 2.68 V typical	–	f_{OSC}/2	–	–
		V_{VREG} ≥ 2.68 V typical	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup Enable Delay Time [2]	$t_{HIC(EN)}$		–	230	–	µs
Hiccup Recovery Time [2]	$t_{HIC(REC)}$		–	930	–	µs
Hiccup OCP PWM Counts	$t_{HIC(OCP)}$	V_{VREG} < 1.3 V_{TYP}, V_{COMP} = $V_{O(EA,MAX)}$	–	32	–	PWM cycles
		V_{VREG} > 1.3 V_{TYP}, V_{COMP} = $V_{O(EA,MAX)}$	–	120	–	PWM cycles
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	$I_{LIM(ton,min)}$	V_{VIN} < 8.5 V	3.83	4.2	4.77	A
		V_{VIN} > 9.5 V	2.49	2.8	3.11	A
LX Short-Circuit Current Limit	$I_{LIM(LX)}$	Latched fault after 2nd detection	5.3	7.1	–	A

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MISSING ASYNCHRONOUS DIODE (D1) PROTECTION						
Detection Level	$V_{D(OPEN)}$		−1.9	−1.4	−1.0	V
Time Filtering [2]	$t_{D(OPEN)}$		50	–	250	ns
VUC, V5A, V5Px LINEAR REGULATORS						
VUC Accuracy and Load Regulation (5 V_{OUT})	V_{VUC5}	10 mA < I_{VUC} < 375 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
VUC Accuracy and Load Regulation (3.3 V_{OUT})	V_{VUC33}	10 mA < I_{VUC} < 375 mA, V_{VREG} = 5.25 V	3.23	3.30	3.37	V
VUC Output Capacitance Range [2]	$C_{OUT(VUC)}$		1.0	–	15	µF
V5A Accuracy and Load Regulation	V_{V5A}	5 mA < I_{V5A} < 150 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5A Output Capacitance Range [2]	$C_{OUT(V5A)}$		1.0	–	15	µF
V5Px Accuracy and Load Regulation	V_{V5Px}	5 mA < I_{V5Px} < 120 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5Px Output Capacitance Range [2]	$C_{OUT(V5Px)}$		1.0	–	15	µF
VUC OVERCURRENT PROTECTION						
VUC Current Limit [1]	$I_{VUC(LIM)}$		–412	–625	–880	mA
VUC Foldback Current [1]	$I_{VUC(FBK)}$	V_{VUC} = 0 V	–65	–187	–275	mA
V5A OVERCURRENT PROTECTION						
V5A Current Limit [1]	$I_{V5A(LIM)}$		–160	–235	–325	mA
V5A Foldback Current [1]	$I_{V5A(FBK)}$	V_{V5A} = 0 V	–20	–78	–163	mA
V5Px OVERCURRENT PROTECTION						
V5Px Current Limit [1]	$I_{V5Px(LIM)}$		–135	–230	–350	mA
V5Px Foldback Current [1]	$I_{V5Px(FBK)}$	V_{V5Px} = 0 V	–20	–60	–125	mA

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VUC, V5A, AND V5Px STARTUP TIMING						
VUC Startup Time (5 V_{OUT}) [2]	$t_{VUC5(START)}$	C_{VUC} = 2.2 µF ±20%, Load = 15 Ω ±10%	–	0.15	1.0	ms
VUC Startup Time (3.3 V_{OUT}) [2]	$t_{VUC33(START)}$	C_{VUC} = 2.2 µF ±20%, Load = 10 Ω ±10%	–	0.13	0.65	ms
V5A Startup Time [2]	$t_{V5(START)}$	C_{V5A} = 2.2 µF ±20%, Load = 40 Ω ±10%	–	0.22	1.2	ms
V5Px Startup Time [2]	$t_{V5Px(START)}$	C_{V5Px} = 2.2 µF ±20%, Load = 50 Ω ±10%	–	0.22	1.2	ms
IGNITION ENABLE (ENBAT) INPUT						
ENBAT Upper Threshold	$V_{ENBAT(H)}$	V_{ENBAT} rising	2.7	3.1	3.5	V
ENBAT Lower Threshold	$V_{ENBAT(L)}$	V_{ENBAT} falling	2.2	2.6	2.9	V
ENBAT Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENBAT(H)} – V_{ENBAT(L)}$	–	500	–	mV
ENBAT Bias Current [1]	$I_{ENBAT(BIAS)}$	V_{ENBAT} = 3.5 V	–	20	50	µA
		V_{ENBAT} = 40 V	–	–	5.5	mA
ENBAT Pulldown Resistance	R_{ENBAT}	V_{ENBAT} < 1.2 V	–	600	–	kΩ
LOGIC ENABLE (ENB) INPUT						
ENB Upper Threshold	$V_{ENB(H)}$	V_{ENB} rising	–	–	2.0	V
ENB Lower Threshold	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Bias Current [1]	$I_{ENB(IN)}$	V_{ENB} = 3.3 V	–	–	175	µA
ENB Resistance	R_{ENB}		–	60	–	kΩ
ENB/ENBAT DELAY						
Enable Falling Delay Time	$t_{dLDO(OFF)}$		10	15	20	µs
VUC, V5A, AND V5Px UNDERVOLTAGE DETECTION THRESHOLDS						
VUC (5 V_{OUT}), V5A, and V5Px Undervoltage Thresholds	$V_{V5(UV,H)}$	V_{V5} rising	–	4.68	–	V
	$V_{V5(UV,L)}$	V_{V5} falling	4.50	4.65	4.80	V
VUC (5 V_{OUT}), V5A, and V5Px Undervoltage Hysteresis	$V_{V5(UV,HYS)}$	$V_{V5(UV,H)} – V_{V5(UV,L)}$	–	30	–	mV
VUC (3.3 V_{OUT}) Undervoltage Thresholds	$V_{3V3(UV,H)}$	V_{3V3} rising	–	3.12	–	V
	$V_{3V3(UV,L)}$	V_{3V3} falling	2.8	3.1	3.19	V
VUC (3.3 V_{OUT}) Undervoltage Hysteresis	$V_{3V3(UV,HYS)}$	$V_{3V3(UV,H)} – V_{3V3(UV,L)}$	–	20	–	mV

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VUC, V5A, V5P1, AND V5P2 OVERVOLTAGE PROTECTION THRESHOLDS						
VUC (5 V_{OUT}), V5A, and V5Px Overvoltage Thresholds	$V_{V5(OV,H)}$	V_{V5A} rising	5.15	5.33	5.5	V
	$V_{V5(OV,L)}$	V_{V5A} falling	–	5.30	–	V
VUC (5 V_{OUT}), V5A, and V5Px Overvoltage Hysteresis	$V_{V5(OV,HYS)}$	$V_{V5A(OV,H)} – V_{V5A(OV,L)}$	–	30	–	mV
V5Px Output Disconnect Threshold	$V_{V5Px(DISC)}$	V_{V5Px} rising	–	7.2	–	V
VUC (3.3 V_{OUT}) Overvoltage Thresholds	$V_{3V3(OV,H)}$	V_{3V3} rising	3.45	3.51	3.66	V
	$V_{3V3(OV,L)}$	V_{3V3} falling	–	3.49	–	V
VUC (3.3 V_{OUT}) Overvoltage Hysteresis	$V_{3V3(OV,HYS)}$	$V_{3V3(OV,H)} – V_{3V3(OV,L)}$	–	20	–	mV
VREG, VCPx, AND BG THRESHOLDS						
VREG Non-Latching Overvoltage Threshold	$V_{VREG(OV,H)}$	V_{VREG} rising, LX PWM disabled	5.70	5.95	6.20	V
	$V_{VREG(OV,L)}$	V_{VREG} falling, LX PWM enabled	–	5.85	–	V
VREG Non-Latching Overvoltage Hysteresis	$V_{VREG(OV,HYS)}$	$V_{VREG(OV,H)} – V_{VREG(OV,L)}$	–	100	–	mV
VREG Undervoltage Thresholds	$V_{VREG(UV,H)}$	V_{VREG} rising, triggers rise of VUC linear regulator	4.50	4.75	5.00	V
	$V_{VREG(UV,L)}$	V_{VREG} falling	–	4.65	–	V
VREG Undervoltage Hysteresis	$V_{VREG(UV,HYS)}$	$V_{VREG(UV,H)} – V_{VREG(UV,L)}$	–	100	–	mV
VCP2 Overvoltage Thresholds	$V_{VCP2(OV,H)}$	Detected on CP2C1 pin. Defined as $V_{VIN} – V_{CP2C1}$, V_{VIN} ≥ 14 V	11.0	12.5	14.0	V
VCP2 Undervoltage Thresholds (Pre-Regulator)	$V_{VCP2(UV,H)}$	V_{VCP2} rising, PWM enabled (w.r.t. V_{VIN})	2.78	3.1	3.26	V
	$V_{VCP2(UV,L)}$	V_{VCP2} falling, PWM disabled (w.r.t. V_{VIN})	–	2.8	–	V
VCP2 Undervoltage Hysteresis	$V_{VCP2(UV,HYS)}$	$V_{VCP2(UV,H)} – V_{VCP2(UV,L)}$	–	400	–	mV
VCP Undervoltage Thresholds	$V_{VCP(UV,H)}$	V_{VCP} rising, PWM enabled (w.r.t. V_{VIN})	5.71	6.3	6.63	V
	$V_{VCP(UV,L)}$	V_{VCP} falling, PWM disabled (w.r.t. V_{VIN})	–	5.1	–	V
VCP Undervoltage Hysteresis	$V_{VCP(UV,HYS)}$	$V_{VCP(UV,H)} – V_{VCP(UV,L)}$	–	1.2	–	V
BG1 and BG2 Undervoltage Thresholds [2]	$V_{BGx(UV)}$	V_{BG1} or V_{BG2} falling	1.00	1.05	1.10	V
OVERVOLTAGE FILTERING/DEGLITCH TIME						
Overvoltage Detection Delay [2]	$t_{d(OV)}$	Overvoltage detection delay time	5	–	25	µs
UNDERVOLTAGE FILTERING/DEGLITCH TIME						
Undervoltage Filter/Deglitch Times [2]	$t_{d(UV)}$	Undervoltage detection delay time	5	–	25	µs

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR TURN-ON AND TURN-OFF DELAYS						
NPOR Turn-On Delay	$t_{d(NPOR,ON)}$	Time from VUC > $V_{3V3(UV,H)}$ (or $V_{V5(UV,H)}$) to when the NPOR pin becomes high impedance	3.7	5	6.3	ms
NPOR OUTPUT VOLTAGES						
NPOR Output Low Voltage	$V_{NPOR(L)}$	I_{NPOR} = 4 mA	–	150	400	mV
		V_{VIN} = 5.5 V, I_{NPOR} = 2 mA	–	–	200	mV
NPOR Leakage Current [1]	$I_{NPOR(LKG)}$	V_{NPOR} = 3.3 V	–	–	2	µA
NPOR ONE-SHOT TIME (ONLY if enabled via SPI using the NPOR_KEY)						
NPOR One-Shot "Low" Time After Watchdog Fault	$t_{WD(FAULT)}$		1.6	2	2.4	ms
FAULT FLAG OUTPUT VOLTAGES (FFn)						
FFn Output Voltage	$V_{FFn(L)}$	FFn is tripped, I_{FFn} = 2 mA	–	150	400	mV
FFn Leakage Current	$I_{FFn(LKG)}$	V_{FFn} = 3.3 V	–	–	2	µA
WD_{IN} VOLTAGE THRESHOLDS AND RESISTANCE						
WD_{IN} Upper Threshold	$V_{WDIN(HI)}$	V_{WDIN} rising	–	–	2.0	V
WD_{IN} Lower Threshold	$V_{WDIN(LO)}$	V_{WDIN} falling	0.8	–	–	V
WD_{IN} Pull-Down Resistance [2]	R_{WDIN}		–	50	–	kΩ
WD TIMING SPECIFICATIONS						
Watchdog Configuration Time	$t_{CONFIG(WD)}$	Can be bypassed by setting WD_SEL bits	–	1000	–	ms
WD_Fn OUTPUT SPECIFICATIONS						
Output Low Voltage	$V_{WD_Fn(L)}$	I_{WD_Fn} = 4 mA	–	150	400	mV
		V_{VIN} = 5.5 V, I_{WD_Fn} = 1 mA	–	–	200	mV
Leakage Current	$I_{WD_Fn(LKG)}$	V_{WD_Fn} = 3.3 V	–	–	2	µA
GATE DRIVE ENABLE (POE)						
POE Output Voltage	$V_{POE(L)}$	I_{POE} = 4 mA	–	150	400	mV
	$V_{POE(H)}$	I_{POE} = –1.5 mA	0.8 × V_{VUC}	–	–	V

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SERIAL INTERFACE (STRn, SDI, SDO, SCK)						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}	All logic inputs	2.0	–	–	V
Input Hysteresis	V_{Ihys}	All logic inputs	250	550	–	mV
MOSI and SCK Input Pull-Down	R_{PD}	V_{MOSI} or V_{SCK} = 3.3 V	–	50	–	kΩ
CS Input Pull-Up to 3.0 V	R_{PU}		–	50	–	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA [1]	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –1 mA [1]	0.8 × V_{VUC}	–	–	V
SPI Clock Frequency [2]	f_{SCK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Frame Rate [2]	t_{SPI}		2.94	–	294	kHz
Clock High Time	$t_{SCK(H)}$	A in Figure 1	40	–	–	ns
Clock Low Time	$t_{SCK(L)}$	B in Figure 1	40	–	–	ns
Chip Select Lead Time	$t_{CS(LD)}$	C in Figure 1	30	–	–	ns
Chip Select Lag Time	$t_{CS(LG)}$	D in Figure 1	30	–	–	ns
Chip Select High Time	$t_{CS(H)}$	E in Figure 1	300	–	–	ns
Data Out (MISO) Enable Time [2]	$t_{MISO(EN)}$	F in Figure 1	–	–	40	ns
Data Out (MISO) Disable Time [2]	$t_{MISO(D)}$	G in Figure 1	–	–	30	ns
Data Out (MISO) Valid Time From SCK Falling [2]	$t_{MISO(V)}$	H in Figure 1	–	–	40	ns
Data Out (MISO) Hold Time From SCK Falling [2]	$t_{MISO(H)}$	J in Figure 1	5	–	–	ns
Data In (MOSI) Set-Up Time To SCK Rising	$t_{MOSI(SU)}$	K in Figure 1	15	–	–	ns
Data In (MOSI) Hold Time From SCK Rising	$t_{MOSI(H)}$	L in Figure 1	10	–	–	ns

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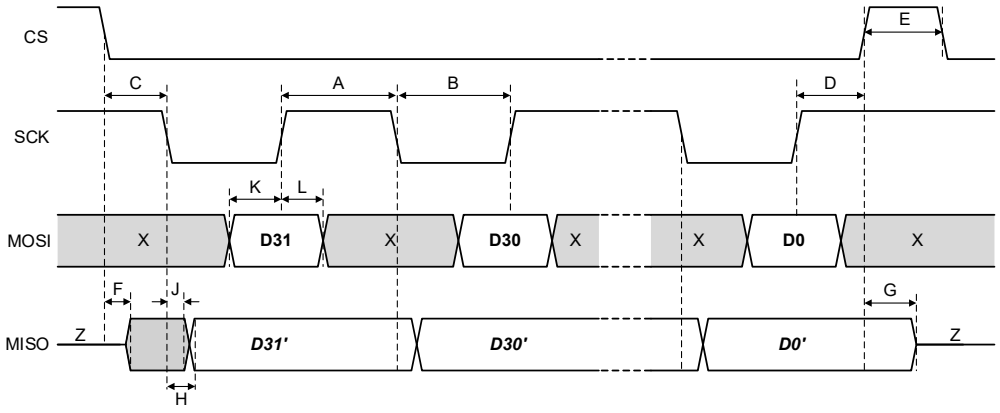

Figure 1: Serial Interface Timing for Write and Read Cycles
MISO activity assumes the Chip_ID from the previous frame was correct

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE (z = U, V, W)						
Turn-On Time	t_r	C_{LOAD} = 10 nF, 20% to 80%	–	5	–	µs
Turn-Off Time	t_f	C_{LOAD} = 10 nF, 80% to 20%	–	0.5	–	µs
Turn-On Pulse Current	I_{GP}		8.5	10	12.5	mA
Turn-On Pulse Time	t_{GP}		22	–	42	µs
On Hold Current	I_{GH}		–	400	–	µA
Pull-Down On Resistance [3]	$R_{DS(on)DN}$	T_J = 25°C, I_G = 10 mA	–	5	–	Ω
		T_J = 150°C, I_G = 10 mA	–	10	–	Ω
Gz and G_{VBB} High Output Voltage	V_{GH}	V_{VIN} > 5.5 V (w.r.t. V_S, or VIN if V_S > V_{VIN})	8	9	12	V
		4.5 V < V_{VIN} ≤ 5.5 V (w.r.t. V_S, or VIN if V_S > V_{VIN}), Buck-Boost mode	7.2	9	–	V
Gz and G_{VBB} Low Output Voltage	V_{GL}	–10 µA < I_G < 10 µA	–	–	V_S + 0.3	V
Gz and G_{VBB} Passive Pull-Down	R_{GPD}	V_G – V_S < 0.3 V	–	950	–	kΩ
Gz and G_{VBB} External Load Resistance [2]	R_G	Between gate and source (using ±1% resistor)	100	–	–	kΩ
GATE DRIVE DIAGNOSTICS AND FILTERING (z = U, V, W)						
Gz and G_{VBB} UV Threshold Rising	$V_{G(UV,H)}$	V_G rising (w.r.t. V_S)	6.0	–	7.1	V
Gz and G_{VBB} UV Threshold Hysteresis [2]	$V_{G(UV,HYS)}$		–	250	–	mV
Gz and G_{VBB} OV Threshold Falling	$V_{G(OV,L)}$	V_G falling (w.r.t. V_S)	0.35	–	1.05	V
Gz and G_{VBB} OV Threshold Hysteresis [2]	$V_{G(OV,HYS)}$		–	150	–	mV
Gz and G_{VBB} Rising/Falling Filter Time	$t_{dFILT(Gz)}$	Voltage detection delay, GD_UV_SEL = 0	–	1.4	–	ms
		Voltage detection delay, GD_UV_SEL = 1	15	20	25	µs
GATE DRIVE PROPAGATION DELAYS (z = U, V, W)						
EN_{VBB} Enable/Disable Delay Times, *GD_EN_SEL = 0*	$t_{d(EN,VBB)}$	From "SPI command is written" to G_{VBB} 20% (enable), to G_{VBB} 80% (disable)	–	1.5	–	ms
ENz Enable/Disable Delay Times, *GD_EN_SEL = 0*	$t_{d(Enz)}$	From "SPI command is written" to Gz 20% (enable), to Gz 80% (disable)	–	10	–	ms
ENVBB and Enz Enable/Disable Delay Times, *GD_EN_SEL = 1*	$t_{d(EN,VBB)}$, $t_{d(Enz)}$	From "SPI command is written" to Gz or G_{VBB} 20% (enable), to Gz or G_{VBB} 80% (disable)	–	–	6	µs
SVBB DIAGNOSTICS AND FILTERING						
SVBB UV Threshold Falling	$V_{SVBB(UV,L)}$	V_{SVBB} falling (w.r.t. GND)	–	2.5	3.0	V
SVBB UV Threshold Hysteresis	$V_{SVBB(UV,HYS)}$		–	650	–	mV
SVBB UV Filter/Deglitch Times	$t_{d(FILT,VBB)}$	Undervoltage detection delay, *GD_UV_SEL = 0*	–	0.8	1.0	ms
		Undervoltage detection delay, *GD_UV_SEL = 1*	15	20	25	µs

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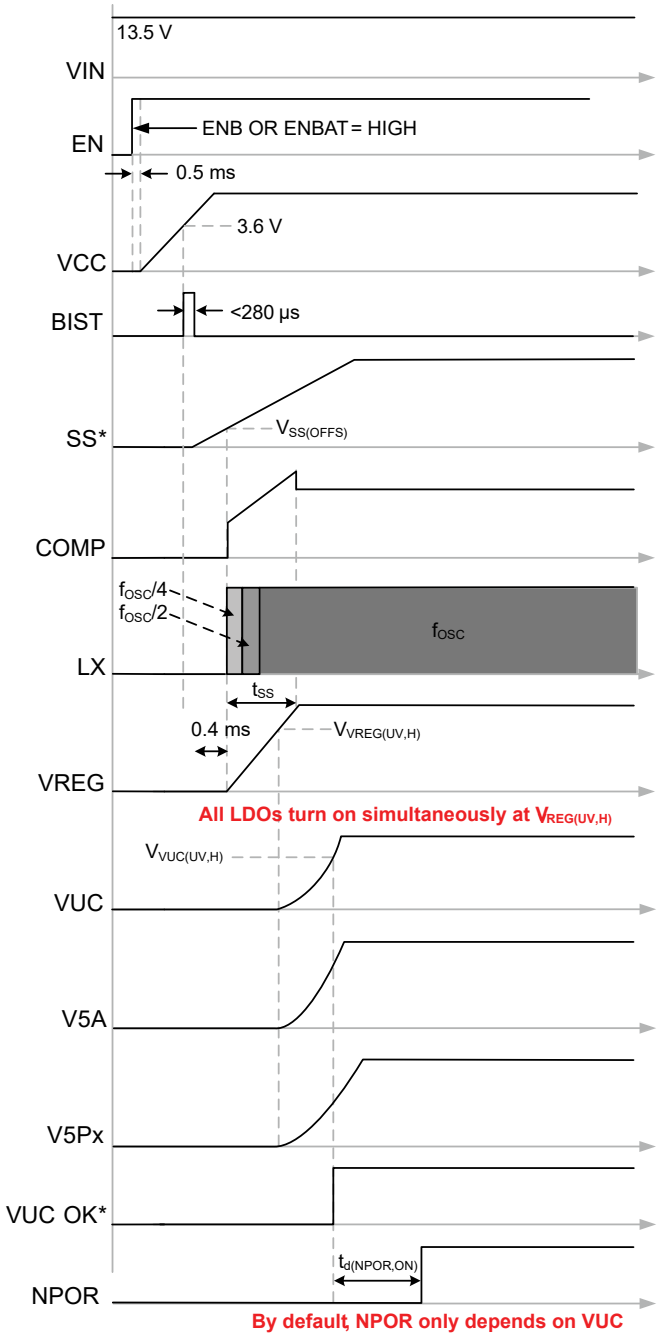

Figure 2: Startup Timing Diagram

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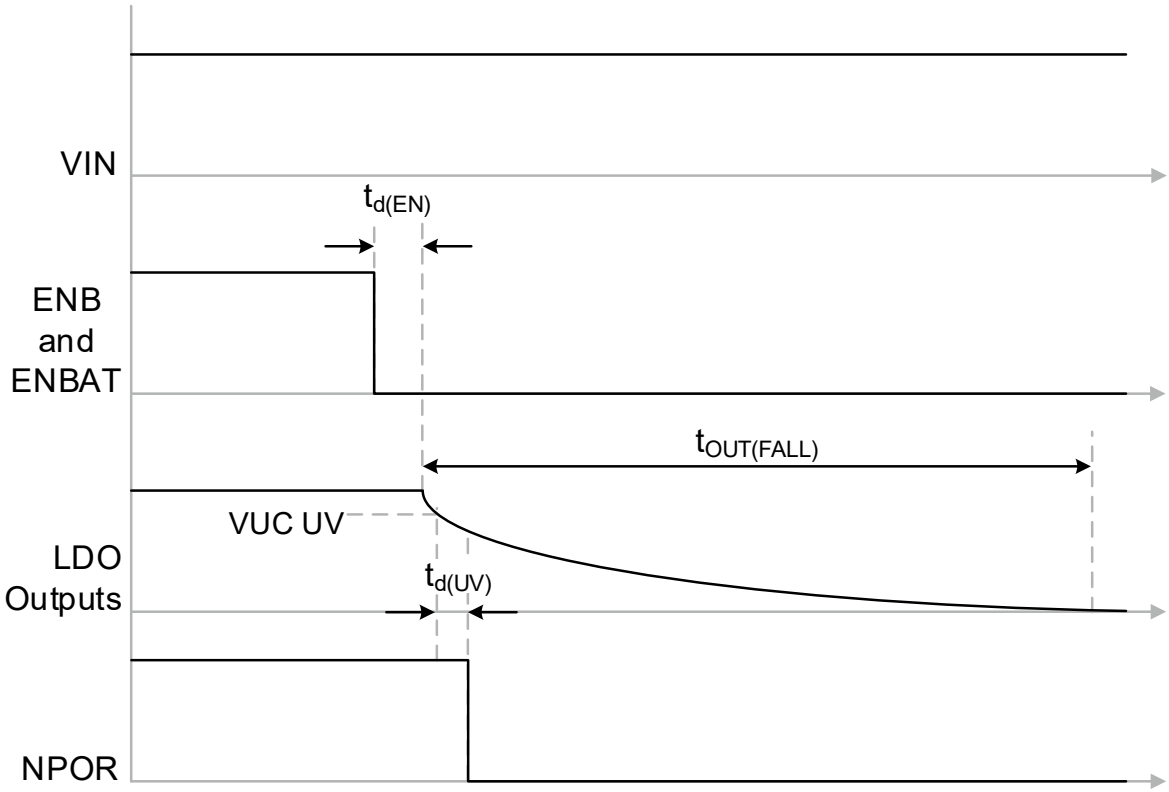

All LDO outputs start to decay $t_{d(EN)}$ seconds after ENB and ENBAT are low.
The time for an output to decay to zero, $t_{OUT(FALL)}$, varies for each LDO and depends on load and output capacitance.
NPOR transitions low after VUC crosses its UV threshold

Figure 3: Shutdown Timing Diagram

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TIMING DIAGRAMS (not to scale)
* is for internal signal or threshold

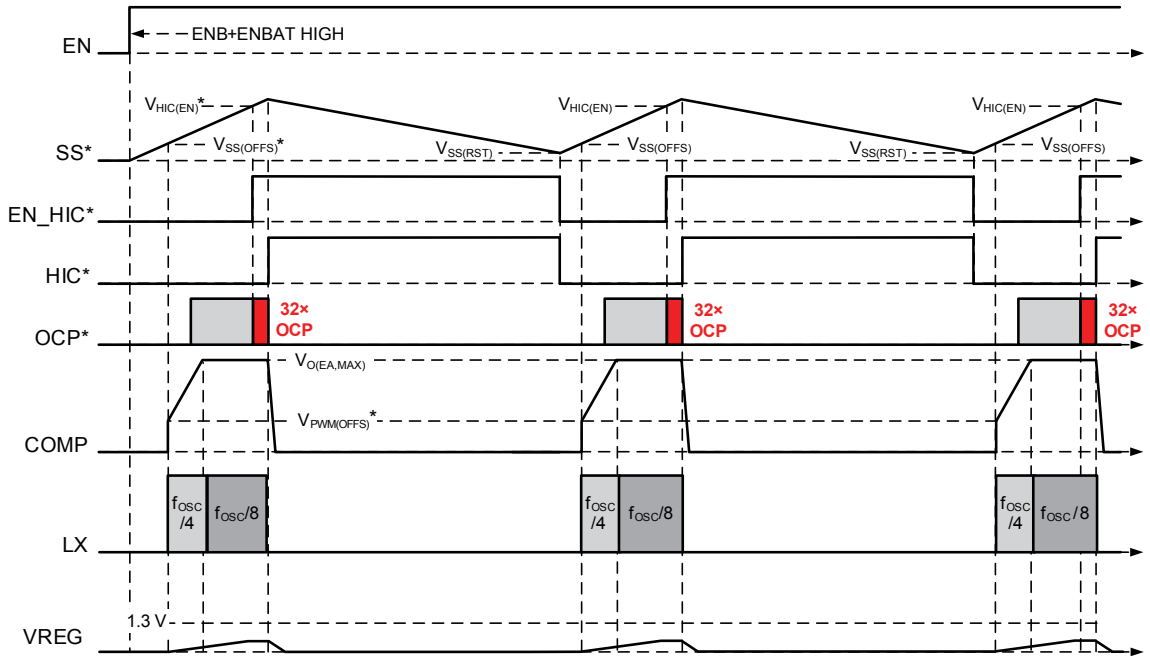

Figure 4: Hiccup Mode Operation with VREG Shorted to GND (R_{LOAD} < 50 mΩ)

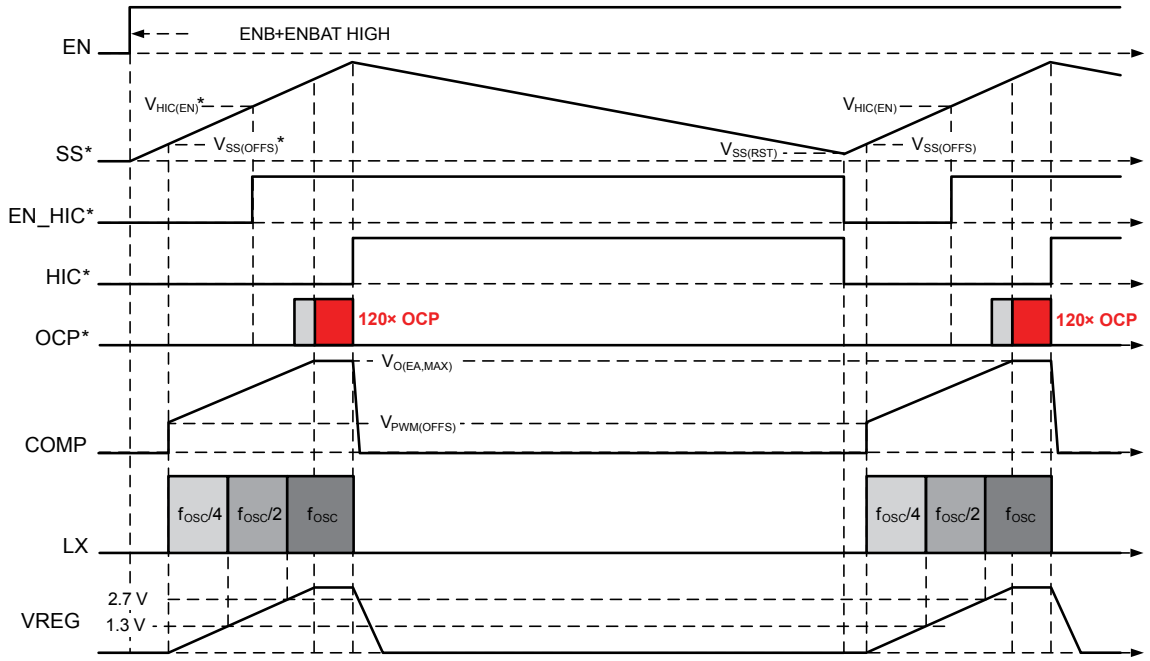

Figure 5: Hiccup Mode Operation with VREG Overloaded (R_{LOAD} ≈ 0.5 Ω)

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Table 1: Summary of Fault Mode Operation

FAULT	A81407 RESPONSE	VREG	VUC	V5A	V5Px [4]	FFn	NPOR	WD_Fn	POE	GVBB	GZ [4]	SPI	WD	RESET
VIN UV	MPOR, VCP2_UV & VCP_UV	0 V	0 V	0 V	0 V	Low	Low	High	Low	Off	Off	Off	Off	Increase VIN
BG1, BG2 UV														Replace the IC
VREG UV	UV by only a small amount, but VUC OK	UV	–	–	–	Low	–	–	–	–	–	On	On	
VUC UV		–	UV	–	–	Low	Low	–	Low	Off	On [9]	On	On	
V5A UV		–	–	UV	–	Low	– [5]	–	–	–	–	On	On	
V5PX UV [4]		–	–	–	UV	Low	–	–	–	–	–	On	On	
VCP2 UV	VCP2_UV & VCP_UV	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On	
VCP UV	No external gate drive	–	–	–	–	Low	–	–	–	Off	Off	On	On	
SVBB_UV	GVBB off to protect FET	–	–	–	–	Low	–	–	–	Off	On [9]	On	On	
G_Z_UV [4] or G_{VBB}_UV when set to ON	Inform the microcontroller	–	–	–	–	Low	–	–	–	–	–	On	On	
G_Z_OV [4] or G_{VBB}_OV when set to OFF	Inform the microcontroller	–	–	–	–	Low	–	–	–	–	–	On	On	
VREG OV		OV	–	–	–	Low	–	–	–	–	–	On	On	
VUC OV		–	OV	–	–	Low	Low	–	Low	Off	On [9]	On	On	
V5A OV		–	–	OV	–	Low	–	–	–	–	–	On	On	
V5Px OV/STB [3][4]	Disconnect occurs >7.2 V	–	–	–	OV [10]	Low	–	–	–	–	–	On	On	
VCP2 OV		0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	On	On	
VCC STG [3]	VCC ILIM and MPOR	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	Off	Remove STG
VREG STG [3]	Hiccup mode	HIC	0 V	0 V	0 V	Low	Low	–	Low	Off	On [9]	Off	On	
VUC STG [3]	VUC Foldback ILIM	–	0 V	–	–	Low	Low	–	Low	Off	On [9]	Off	On	
V5A STG [3]	V5A Foldback ILIM	–	–	0 V	–	Low	–	–	–	–	–	On	On	
V5PX STG [3]	V5PX Foldback ILIM	–	–	–	0 V	Low	–	–	–	–	–	On	On	
LX STG [3]	Latch off after 2×	Off	0 V	0 V	0 V	Low	Low	–	Low	Off	On [9]	Off	On	
LG STG [3]	V_{VIN} > 8.5 V, LG off	–	–	–	–	–	–	–	–	–	–	On	On	
	V_{VIN} < 8.5 V, LG active	–	–	–	–	Low	–	–	–	–	–	On	On	
VCP2 STG [3]	VCP2 high current and fusing. Definitely VCP_UV too.	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On or Off	Replace the IC
VCP STG [3]	VCP high current and fusing, no external gate drive. Likely VCP2_UV too.	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On or Off	
CP2C1 STG [3]	VCP2_UV and VCP_UV	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On	Remove STG
CP2C2 STG [3]	VCP2 high current and fusing	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On	Replace the IC
CP1 STG [3]	VCP high current and fusing, no external gate drive. Likely VCP2_UV too.	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On or Off	Remove STG
CP2 STG [3]	VCP high current and fusing	–	–	–	–	Low	–	–	–	Off	Off	On	On	Replace the IC
Watchdog Fault	PWWD, WWD, or Q&A	–	–	–	–	– [6]	– [7]	Low	Low	– [8]	– [8]	On	On	
BIST Fault	Inform the microcontroller	–	–	–	–	Low	–	–	–	–	–	On	On	
DBE Fault	Inform the microcontroller	–	–	–	–	Low	–	–	–	–	–	On	On	
SE Fault	Inform the microcontroller	–	–	–	–	Low	–	–	–	–	–	On	On	
L1 missing	VREG cannot rise	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	On [9]	Off	On	Replace missing component, or remove short circuit.
Diode D1 missing	Latch off after 2×	Off	0 V	0 V	0 V	Low	Low	–	Low	Off	On [9]	Off	On	
$C_{CP2C1/CP2C2}$ missing	VCP2_UV and VCP_UV	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On	
C_{VCP2} missing	VCP2_UV & VCP_UV	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On	
$C_{CP1/CP2}$ missing	VCP2_UV, No ext. gate drive	–	–	–	–	Low	–	–	–	Off	Off	On	On	
C_{VCP} missing	VCP2_UV, No ext. gate drive	–	–	–	–	Low	–	–	–	Off	Off	On	On	
L1 shorted	LX fault, latch off after 2×	Off	0 V	0 V	0 V	Low	Low	–	Low	Off	On [9]	Off	On	
$C_{CP2C1/CP2C2}$ shorted	VCP2_UV and VCP_UV	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On	
C_{VCP2} shorted	VCP2_UV & VCP_UV	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	Off	Off	On	
$C_{CP1/CP2}$ shorted	VCP_UV, No ext. gate drive	–	–	–	–	Low	–	–	–	Off	Off	On	On	
C_{VCP} shorted	VCP_UV, No ext. gate drive	–	–	–	–	Low	–	–	–	Off	Off	On	On	
TSD	Stop PWM, maintain SPI	0 V	0 V	0 V	0 V	Low	Low	–	Low	Off	On [9]	Off	On	IC cooldown

[1] "–" = No effect, operates normally.

[2] MPOR = Master Power-On Reset.

[3] STG = short-to-ground, STB = short-to-battery.

[4] V5Px where (x = 1 or 2), G_Z where (z = U or V or W).

[5] By default, V5A UV will not affect NPOR. However, there is an option, via SPI programming, to have NPOR transition low if V5A is UV.

[6] By default, a WD Fault will not affect FFn. However, there is an option, via SPI programming, to have FFn latch low.

[7] By default, a WD Fault will not affect NPOR. However, there is an option, via SPI programming, to have NPOR momentarily transition low for 2 ms to reset the MCU.

[8] By default, a WD Fault will not affect the four gate drivers. However, there is an option, via WDF_2_Gz, to have all four gate drivers turn off after a watchdog fault.

[9] By default, the state of GVBB is off and GU/GV/GW are on after a fault, other than a watchdog fault. However, there is an option, via GD_FLT_ON, to have GU/GV/GW turn off.

[10] V5Px STB will be reported to SPI diagnostic register (0x05) as both V5Px UV and OV fault.

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FUNCTIONAL DESCRIPTION

Overview

The A81407 pre-regulator can be configured as an asynchronous buck or buck-boost converter. This pre-regulator generates a fixed 5.35 V (VREG) and can deliver up to 1.2 A to power the internal post-regulators. The post regulators generate the various voltage levels for the end system.

Pre-Regulator (VREG)

The pre-regulator incorporates an internal high-side and a boost switch gate driver. An external free-wheeling diode and LC filter are required to complete the buck converter. By adding a MOSFET and boost diode, the pre-regulator can maintain all outputs with input voltages down to 3.8 V.

The pre-regulator provides many protection and diagnostic functions:

1. Pulse-by-pulse and hiccup mode current limit
2. Undervoltage and overvoltage detection and reporting
3. Shorted switch node to ground protection
4. Open free-wheeling diode (D1) protection
5. High voltage rating for load dump

PWM Switching Frequency

The switching frequency of the A81407 is fixed at 2.2 MHz, typical. The A81407 includes a frequency foldback scheme that starts when V_{VIN} is greater than 18 V. From 18 to 36 V, the switching frequency will foldback from 2.2 to 1 MHz (typical). The switching frequency (f_{SW}) for a given input voltage (V_{VIN}) above 18 V and below 36 V is:

$$f_{SW} \text{ in MHz} = 3.4 - (1.2 / 18) \times V_{VIN}$$

Bias Supply (VCC)

The bias supply (V_{CC}) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure safe operation of the A81407. These features include:

1. VIN input undervoltage lockout
2. VCC undervoltage detection
3. VCC overcurrent and short-circuit current limit
4. Dual input operation: VIN or VREG, for ultra-low battery voltage operation

Charge Pump (VCP, VCP2)

Charge pump circuits provide the voltage necessary to drive high-side N-channel MOSFETs in the pre-regulator, linear regulators, and floating gate drivers. Four external capacitors are required for charge pump operation. During the first cycle of the charge pump, the flying capacitor between pins CP2C1 and CP2C1 is charged from either VIN or VREG, whichever is highest. During the second cycle, the voltage on the flying capacitor charges the VCP2 capacitor and the flying capacitor between CP1 and CP2. During the last cycle, the voltage on the flying capacitor charges the VCP capacitor. The charge pump incorporates some safety features:

1. Undervoltage and overvoltage detection and reporting
2. Overcurrent safe mode protection

Bandgap (BG1, BG2)

Dual band gaps are implemented within the A81407. One bandgap is dedicated to the voltage regulation loops within each of the regulators, VCC, VCP, VCP2, VREG, and the four post regulators. The second is dedicated to the undervoltage and overvoltage monitoring functions of all the regulators. This improves safety coverage and fault reporting from the A81407.

Should the regulation bandgap fail, then the output voltages will be out of specification and the monitoring bandgap will report the fault.

If the monitoring bandgap fails, the output voltages will remain in regulation, but the monitoring circuits will report the outputs as out of specification and trip the fault flag.

The bandgap circuits include two smaller, secondary bandgaps that are used to monitor the undervoltage state of the main bandgaps.

Enable Inputs (ENB, ENBAT)

Two enable pins are available on the A81407. A high signal on either of these pins enables the regulated outputs of the A81407. One enable (ENB), is logic level compatible. The second enable (ENBAT), is battery-level rated and can be connected to the ignition switch through a low-pass filter.

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Linear Regulators

The A81407 has four linear regulators: one (VUC) that provides 3.3 V (or 5 V for the A81407-1), and three fixed at 5 V (V5A, V5P1, V5P2). Two of these regulators (V5P1, V5P2) are high-voltage tolerant so they are protected from connection to the battery voltage. This makes these outputs most suitable for powering remote sensors or circuitry where a short-to-battery is possible.

The pre-regulator supplies 5.35 V (VREG) to the linear regulators, which reduces power dissipation and temperature.

All linear regulators provide the following protection features:

1. Current limit with foldback
2. Undervoltage and overvoltage detection and reporting

Fault Detection and Reporting (NPOR, WD_Fn, FFn)

There is extensive fault detection within the A81407; most have been discussed previously. There are two fault reporting mechanisms used by the A81407; one through hardwired pins and the other through serial communications interface (SPI).

Three hardwired pins are used for fault reporting. The first pin, NPOR (open-drain, active low), reports on the status of the VUC output. By default, this signal transitions low only if VUC is out of regulation (undervoltage or overvoltage). However, options are available to: (1) report a Watchdog Fault by momentarily setting NPOR low for 2 ms, and (2) indicate if V5A is out of regulation. These additional NPOR options are selectable through SPI.

The second pin, WD_Fn (open-drain, active low), latches low if a Watchdog Fault is detected.

A third pin, FFn (open-drain, active low), reports on all other faults. FFn transitions low when a fault is detected. The FFn output should be connected to an interrupt pin on the processor so it will check the A81407 status and take appropriate action if a fault occurs. By default, FFn does not report a Watchdog Fault, but it may be added to the FFn logic via SPI programming.

Safe State Control Signal (POE)

The safe state control signal or power-on enable (POE) is a signal generated when certain potentially unsafe failures occur. The A81407 is designed to power a system microcontroller with its VUC output. It can also monitor this system controller using a watchdog function. A failure of the system controller may be considered to be unsafe. The following faults will cause the POE signal to be low:

1. Watchdog fault
2. VUC fault

The POE signal can be used to put the system in a safe state, for example, by disabling the gate driver in a motor application.

POE includes some additional safe systems. It is continuously monitored to ensure the signal output matches the A81407 internal circuit's demand. It is also powered by a separate internal power rail for added protection.

Startup Self-Tests

The A81407 includes self-test which is performed during the startup sequence. This self-test verifies the operation of the undervoltage and overvoltage detect circuits for the main outputs, and the overtemperature shutdown circuitry.

In the event the self-test fails, the A81407 will report the failure through SPI.

Undervoltage Detect Self-Test

The undervoltage (UV) detection circuits are verified during startup of the A81407. A voltage that is lower than the undervoltage threshold is applied to each UV comparator; this should cause the corresponding undervoltage bit in the Diagnostic register to change state: 0→1, indicating a fault. If a diagnostic UV register bit does not change state, the corresponding Verify Result bit is latched high. So, when testing is complete, if any bits in the Verify Result registers are high, then verification has failed. The following UV comparators are tested: VREG, VUC, V5A, V5P1, and V5P2.

Overvoltage Detect Self-Test

The overvoltage (OV) detection circuits are verified during startup of the A81407.

A voltage that is higher than the overvoltage threshold is applied to each OV comparator; this should cause the corresponding overvoltage bit in the Diagnostic register to change state: 0→1, indicating a fault. If a diagnostic OV register bit does not change state, the corresponding Verify Result register bit is latched high. So, when testing is complete, if any bits in the Verify Result registers are high then verification has failed. The following OV comparators are tested: VREG, VUC, V5A, V5P1, and V5P2.

Overtemperature Shutdown Self-Test

The overtemperature shutdown (TSD) detector is verified during startup of the A81407.

A voltage that is higher than the overvoltage threshold is applied to the TSD comparator; this should cause the overtemperature bit in the Diagnostic register to change state: 0→1, indicating a fault. If the TSD register bit does not change state, the TSD Verify Result register bit is latched high. So, when testing is complete, if the TSD bit in the Verify Result registers is high, then verification has failed.

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Power-On Enable (POE) Self-Test

The A81407 incorporates continuous self-testing of the power-on enable (POE) output. It compares the status of the POE pin (POE_S) with the internal expected status. If they differ for any reason, the FFn output pin is set low and POE_OK in the status register is set low.

Analog Multiplexer Output

The AMUX pin is the output of an analog multiplexer to monitor the voltages shown in Table 2. The output of the MUX is chosen through SEL_MUX_(3:0) in register 0x09. The accuracy of the MUX is ±6%. The driving capability of this output is 1 mA and the maximum voltage is 3.8 V. Typical response time from writing SEL_MUX_(3:0) to AMUX output change is 20 µs.

Table 2: Analog Multiplexer Output

Node	Signal Divide Ratio	Tolerance (reference)
VREG	1/2	±6%
VUC	1/2	±6%
V5A	1/2	±6%
V5P1	1/2	±6%
V5P2	1/2	±6%
VENBAT	1/8	±6%
VCP	1/12	±6%
VCP2	1/12	±6%
BG1	1/1	±6%
BG2	1/1	±6%
VIN	1/10	±6%
TEMP	–	Output (mV) = 1440 mV – 3.92 mV/°C × T_J (°C)

Floating MOSFET Gate Drivers

The A81407 has four independent floating gate drive outputs to drive external, low on-resistance, power N-channel MOSFETs. These MOSFETs should be connected as a single battery line disconnect (GVBB) and three motor phase isolators (GU, GV, GW). The four gate drivers can be controlled independently through the serial interface by setting the appropriate bit in the control register.

A charge pump (VCP) provides the above-battery supply voltage necessary to maintain the power MOSFETs in the on-state continuously when the phase voltage is equal to the battery voltage.

An internal resistor, R_{GPDz}, between the Gz and Sz pins plus an integrated hold-off circuit, ensures the gate source voltage of each MOSFET is held close to 0 V even with the power disconnected. This can remove the need for additional gate source resistors on the isolation MOSFETs. In any case, if external gate source resistors (R_{GSz}) are mandatory for the application, then the VCP regulator can provide sufficient current to maintain the MOSFET in the on-state with a gate source resistor as low as 100 kΩ.

The floating gate-drive outputs for external N-channel MOSFETs are provided on pins GVBB, GU, GV, and GW. When Gz = 1 (or "high"), the upper half of the driver is on and current will be sourced to the gate of the MOSFET, turning it on. When Gz = 0 (or "low"), the lower half of the driver is on and will sink current from the external MOSFET's gate to the respective Sz terminal, turning it off.

The reference points for the floating drives are the load phase connections, SVBB, SU, SV, and SW. The discharge current from the floating MOSFET gate capacitance flows through these connections.

In some applications, it may be necessary to provide a current recirculation path when the motor load is isolated. This will be necessary in situations where the motor driver does not reduce the load current to zero before the isolation MOSFETs are turned off. The recirculation path can be provided by connecting a suitably rated power diode to the "motor" side of the isolation MOSFETs and GND. See the Functional Block Diagram for more details.

Watchdog Timers

The A81407 contains three different watchdog timers. This section will describe each one in detail. The selection and configuration of each watchdog is done through SPI. After a watchdog is selected and running, it cannot be reconfigured without going through a secure SPI procedure. The watchdog circuits are updated/latched when the state machine leaves the configuration mode. After leaving the CONFIG state, modifications to the watchdog registers will not take effect unless a CONFIG or RESTART command is issued.

The three types of watchdogs are:

1. Pulse Width Watchdog (PWWD) (default)
2. Window Watchdog (WWD)
3. Q&A Watchdog (QAWD)

The Pulse Width Watchdog is the default watchdog. It will automatically start with default settings if the following conditions are met:

1. NPOR transitions high, and
2. No watchdog is selected: WD_SEL_(1:0) = [0,0], and
3. The $t_{CONFIG(WD)}$ configuration timer expires (1000 ms).
   A. The configuration timer can be forced to expire by selecting a watchdog, including the PWWD, with the WD_SEL_(1:0) bits.

A watchdog fault sets pins WD_Fn and POE low. By default, a watchdog fault does not affect NPOR. However, at any time, the microcontroller can select an alternate mode for NPOR after a watchdog fault. This is accomplished by writing three secure words to the NPOR_KEY registers. In the alternate mode, a

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watchdog fault will momentarily set NPOR low for $t_{WD(FAULT)}$ (2 ms) in an attempt to reset/restore the microcontroller.

By default, a watchdog fault does not affect FFn. However, at any time, the microcontroller can modify how FFn behaves after a watchdog fault. If configuration bit WDF_2_FFn is set, then FFn will transition low if it detects a watchdog fault.

By default, a watchdog fault has no effect on the state of the four gate drivers: GVBB, GU, GV, and GW. However, at any time, the microcontroller can modify how the gate drivers behave after a watchdog fault. If configuration bit WDF_2_Gz, in register 0x08, is set, then all four gate drivers will turn off if a watchdog fault occurs.

PULSE WIDTH WINDOW WATCHDOG (PWWD)

The Pulse Width Watchdog circuit monitors an external clock applied to the WD_{IN} pin. This clock should be generated by the primary microcontroller or DSP. The PWWD watchdog measures the time between two clock edges, either rising or falling. So the watchdog effectively measures both the "high" and "low" pulse widths, as shown in Figure 6. By default, the nominal WD_{IN} pulse width (PWWD_PW) is set to 1 ms, but can be modified to 0.5, 1.5, or 2 ms via SPI.

If an incorrect pulse width is detected, the watchdog increments its fault counter by 10 (default). If a correct pulse width is detected, the watchdog decrements its fault counter by 2 (default). If the watchdog fault counter exceeds 160 (default), then both the WD_Fn and POE pins transition low. Operation of the PWWD is shown in Figure 6 and Figure 7. The increment value (PWWD_INC), decrement value (PWWD_DEC), and maximum fault count (PWWD_MAX) all have alternate values that can be accessed via SPI.

The watchdog default values are loaded when:

1. The internal rail, VCC, transitions low (i.e. V_{IN} is removed, or ENB and ENBAT are both low) or
2. The band gap, BG1, transitions low

The watchdog can be restarted by the microcontroller when:

1. The microcontroller sends either a RESTART or CONFIG command via the 3-word WD_KEYs

By default, the PWWD watchdog is enabled after NPOR transitions high and remains high for at least $t_{CONFIG(WD)}$ (1000 ms). This delay should allow ample time for the microcontroller to modify the registers via SPI and begin delivering a clock to the WD_{IN} pin. The $t_{CONFIG(WD)}$ time is shown in Figure 6, Figure 7, and Figure 12. Alternatively, if the microcontroller quickly modifies all registers and generates the WD clock, t_{CONFIG} may be too long. In this case, simply setting WD_SEL_(1:0) ≠ [00] will bypass any remaining t_{CONFIG} time and move the state machine from the CONFIG to the NORMAL state. Both cases are shown in the watchdog state diagram, Figure 12.

Clock pulses from the microcontroller must be applied to WD_{IN} before the watchdog is selected (via WD_SEL) or restarted (via the 3-word WD_KEY command). The PWWD error counter can be preloaded to a value set by PWWD_POE_DLY (default of 2). Preloading the error counter forces the microcontroller to send valid pulses before POE transitions high, effectively "pre-qualifying" the performance of the microcontroller. Figure 6 and Figure 7 demonstrate prequalification with PWWD_POE_DLY set to a value of 10, which requires 5 valid clock pulses (–2 counts per valid clock pulse) before POE transitions high.

After moving into NORMAL operation, if no clock edges are detected at WD_{IN} for PWWD_EDGE_TO, both WD_Fn and POE pins transition low. By default, PWWD_EDGE_TO is 5 ms, but can be modified to 2.5, 10, or 15 ms via SPI. The "edge timeout" condition is shown as (1) in Figure 7.

While in the NORMAL state, if clock activity at WD_{IN} terminates for at least PWWD_ACT_TO, both WD_Fn and POE pins transition low. By default, PWWD_ACT_TO is 16 ms, but can be modified to 8, 24, or 32 ms via SPI. The "loss of clock activity" condition is shown as (2) in Figure 7.

The pulse widths generated by a microcontroller or DSP depend on many factors and will have some pulse-to-pulse variation. The A81407 accommodates pulse width variations by allowing the designer to select a "window" of allowable variations. By default, the window tolerance (PWWD_WIN_TOL) is set to ±13%, but can be modified to ±8, ±18, and ±23 percent via SPI.

The watchdog performs its calculations based on an internally generated clock. The internal clock typically has an accuracy of ±2.5% at 25°C, but may vary as much as ±5% due to IC process shifts and temperature variations. Variations in the watchdog clock result in a shift of the "OK Region" (i.e. the expected pulse width) at WD_{IN}. This is shown as a green, shaded area in Figure 8.

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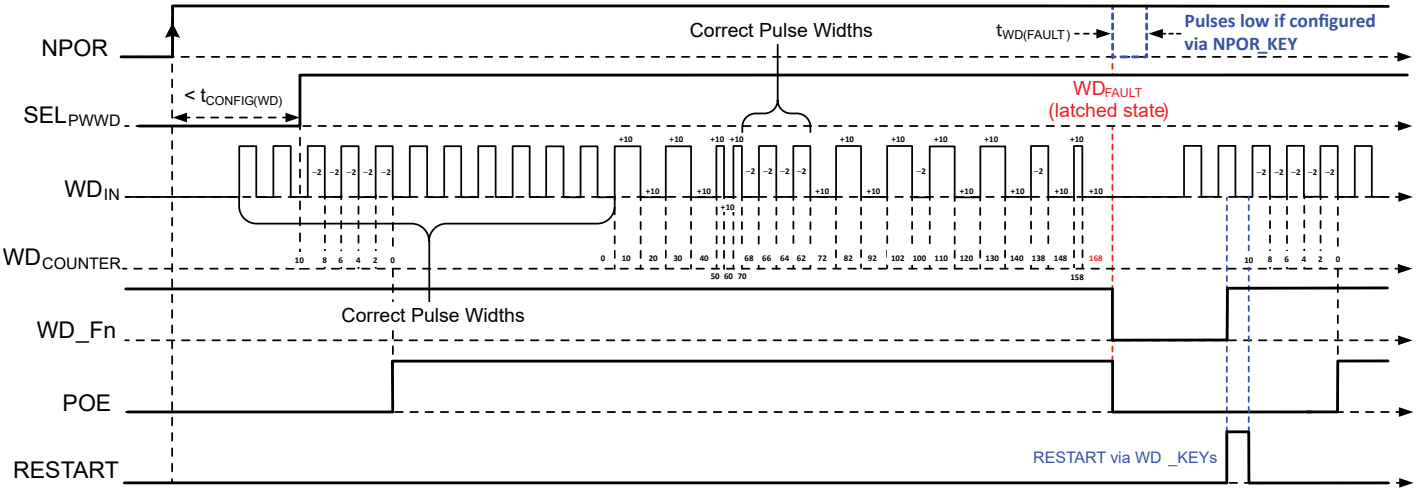

Figure 6: Watchdog (WD) operation with both correct and incorrect pulse widths.

1. Incorrect pulse widths increment the WD counter by 10.
2. Correct pulse widths decrement the WD counter by 2.
3. A WD fault occurs if the total fault count exceeds 160.
4. PWWD_POE_DLY is set to 10. So, 5 valid pulse widths (10 ÷ 2 counts per valid pulse) are required before POE transitions high

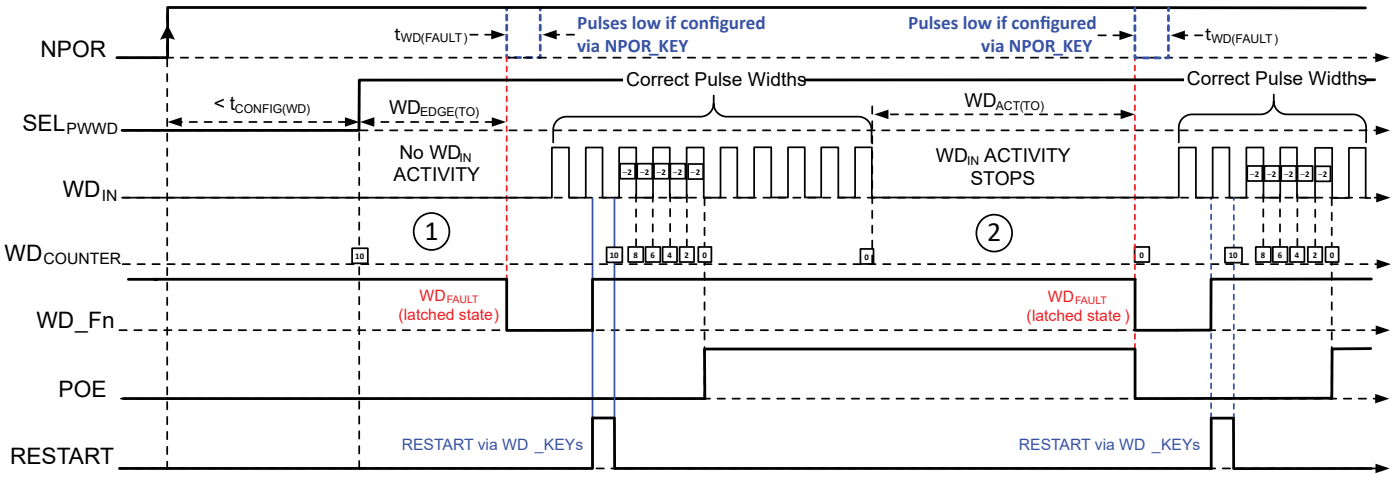

Figure 7: Watchdog operation with faults from:

1. No WD_{IN} Activity for $WD_{EDGE(TO)}$
2. WD_{IN} Activity Stops
3. PWWD_POE_DLY is set to 10.

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PWWD TIMING DIAGRAM (not to scale):

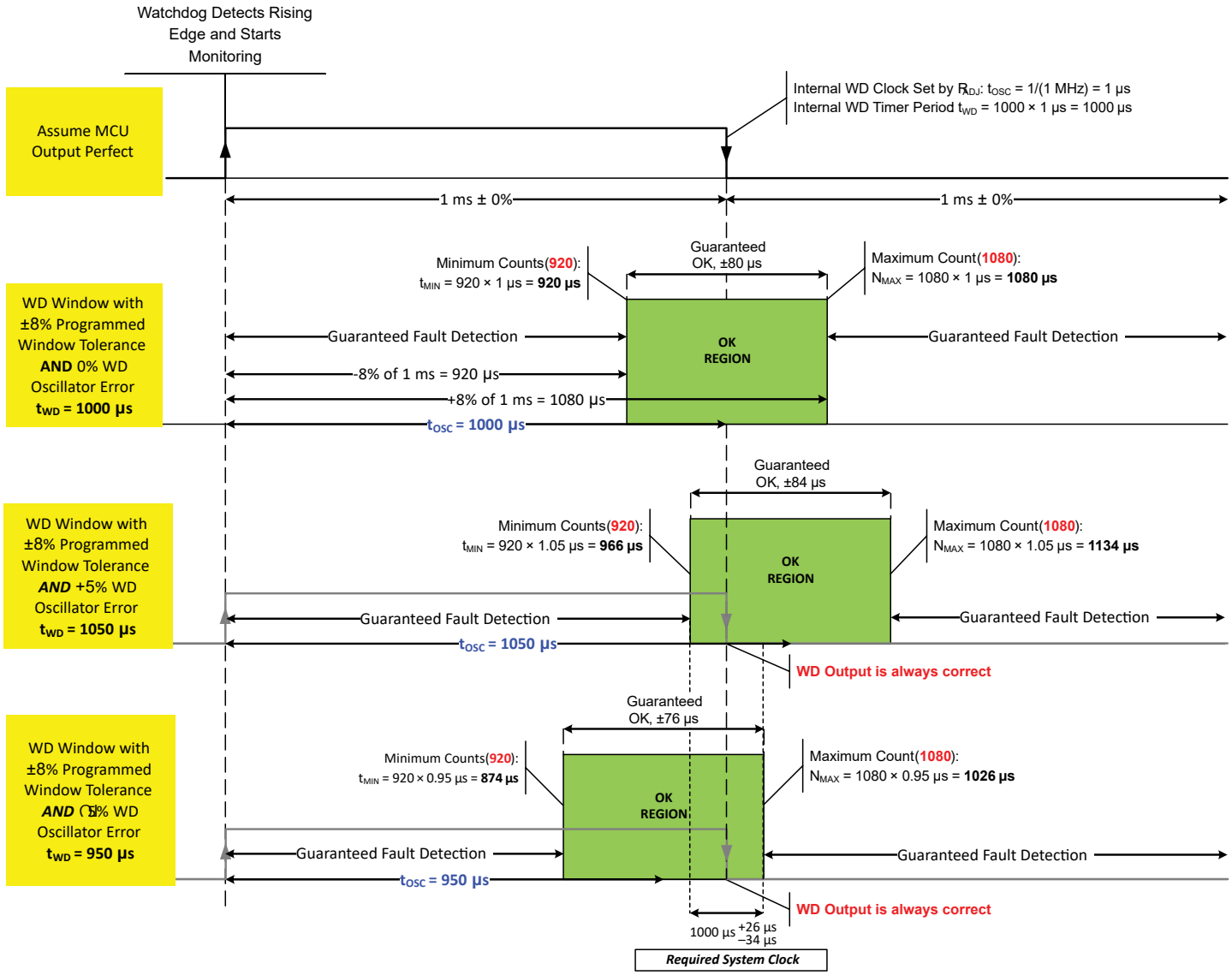

Figure 8: Typical Watchdog Timer System Level Functionality (times are not to scale)

A81407 and System Operating Parameters:

1. 1 ms pulse widths coming from the micro-controller
2. ±8% WD Window Tolerance Selected (WD_{ADJ} = GND)
3. ±5% WD Oscillator Tolerance (worst case maximum)

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WINDOW WATCHDOG (WWD)

The window watchdog monitors the time between rising edges of an external clock applied to the WD_{IN} pin. This clock should be generated by the microcontroller or DSP. The time between rising edges (i.e. the frequency) of the clock must fall within an acceptable "window", or a watchdog fault is generated. In general, valid watchdog clocks must be present at WD_{IN} for at least $t_{WD(SLOW)}$ before POE will transition high.

After NPOR transitions high, the processor must:

1. Program the configuration registers and initiate valid WD pulses on the WD_{IN} pin and,
2. Select the WWD by setting WD_SEL_(1:0) = [10].

Both these tasks must be completed before t_{CONFIG} expires.

A window watchdog fault occurs if the time between rising clock edges is either too short (a "fast" fault) or too long (a "slow" fault). The "fast" and "slow" limits, $t_{WD(FAST)}$ and $t_{WD(SLOW)}$, are selected with WWD_TIMER(2:0). The default values for $t_{WD(FAST)}$ and $t_{WD(SLOW)}$ are 4 ms and 32 ms, respectively.

The options available by WWD_TIMER are 0.5 to 12.5 ms for $t_{WD(FAST)}$, and 4 to 100 ms for $t_{WD(SLOW)}$.

It is strongly recommended that the processor produce valid clock pulses at WD_{IN} prior to selecting the watchdog or issuing a RESTART command. As shown in Figure 9 and Figure 10, after setting WD_SEL(1:0) or issuing a RESTART command, valid watchdog clocks should be present at WD_{IN} for at least $t_{WD(SLOW)}$ before POE is allowed to transition high. This "prequalifies" correct operation of the microcontroller before enabling the gate driver (via POE). At least 1 complete clock cycle must occur during the pre-qualification time ($t_{WD(SLOW)}$). For prequalification, the maximum WD_IN clock frequency ($f_{WD_IN(MAX)}$, including system tolerances) and the selected value of WWD_TIMER from register 0x0A must satisfy the following equation:

$$t_{WD_SLOW} > 1.5 / f_{WD_IN(MAX)}$$

Typical watchdog operation with both FAST and SLOW fault events, along with recommended RESTART conditions, are shown in Figure 9 and Figure 10.

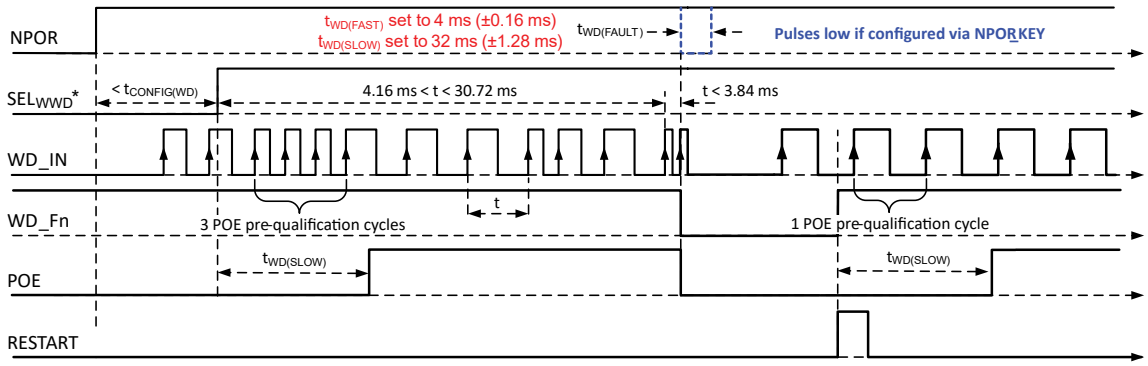

Figure 9: Window Watchdog (WWD) Operation
A watchdog fault occurs when the WD_IN period (T) is too short. * Signal is internal to A81407

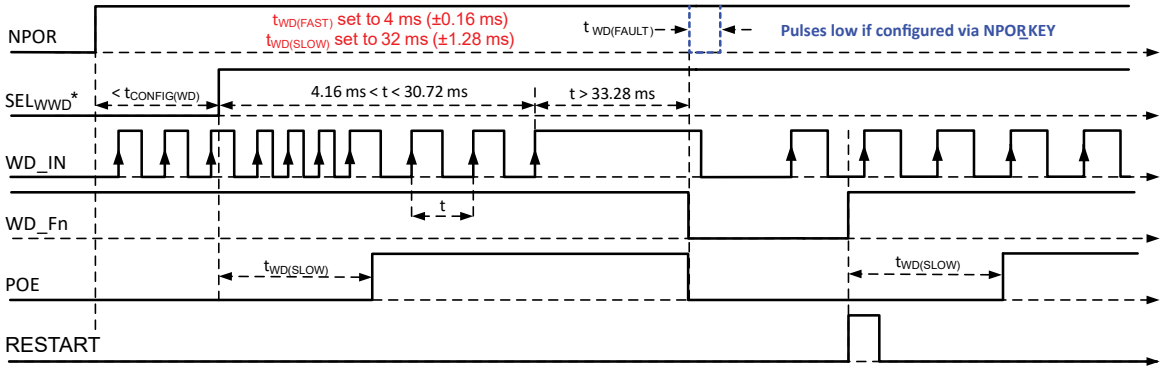

Figure 10: Window Watchdog (WWD) Operation
A watchdog fault occurs when the WD_IN period (t) is too long. * Signal is internal to A81407

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Q&A WATCHDOG

The Q&A watchdog periodically generates a random word and must receive an answer code from the microcontroller or DSP within a specific time window. The Q&A watchdog must be fully configured through SPI before being "activated" with WD_SEL_(1:0). For example, the minimum and maximum time limits ($t_{QA(MIN)}$, $t_{QA(MAX)}$) must be selected from a list of 16 possibilities using QAWD_TIMER_(3:0). Any time POE is low, the microcontroller must successfully complete a Q&A session before POE will transition high.

After the Q&A watchdog is activated, via WD_SEL_(1:0), the A81407 will generate a 6-bit random word, QAWD_RAND_(5:0) and start an internal timer. Shortly thereafter, the microcontroller must synchronize its own timer. Then the microcontroller must read the random word and allow enough time, with margin, to modify and write the word back to the watchdog. The writeback must not occur before the minimum time limit expires ($t_{QA(MIN)}$), nor after the maximum time limit expires ($t_{QA(MAX)}$).

The microcontroller must invert each bit of the random word and wait for the minimum time limit to elapse ($t_{QA(MIN)}$). After the minimum time limit expires, the microcontroller must write the modified word back to QAWD_RAND_(5:0). The write must be fully completed before the maximum time limit expires ($t_{QA(MAX)}$), with margin. Immediately after the writeback occurs, both the Q&A watchdog and the microcontroller must again synchronize their internal timers (i.e. set them to zero and begin counting) to start the next Q&A session.

The microcontroller is allowed to retry the Q&A sequence a number of times before a Watchdog fault is declared. The number of retries can be selected by a 2-bit word, QAWD_RETRY_(1:0). A Q&A Watchdog fault occurs only after the retry counter reaches zero, as shown in Figure 11. The retry counter is decremented if:

1. An answer is received before the minimum time limit expires ($t_{QA(MIN)}$).
2. An answer is not received before the maximum time limit expires ($t_{QA(MAX)}$).
3. An incorrect answer is received from the microcontroller.

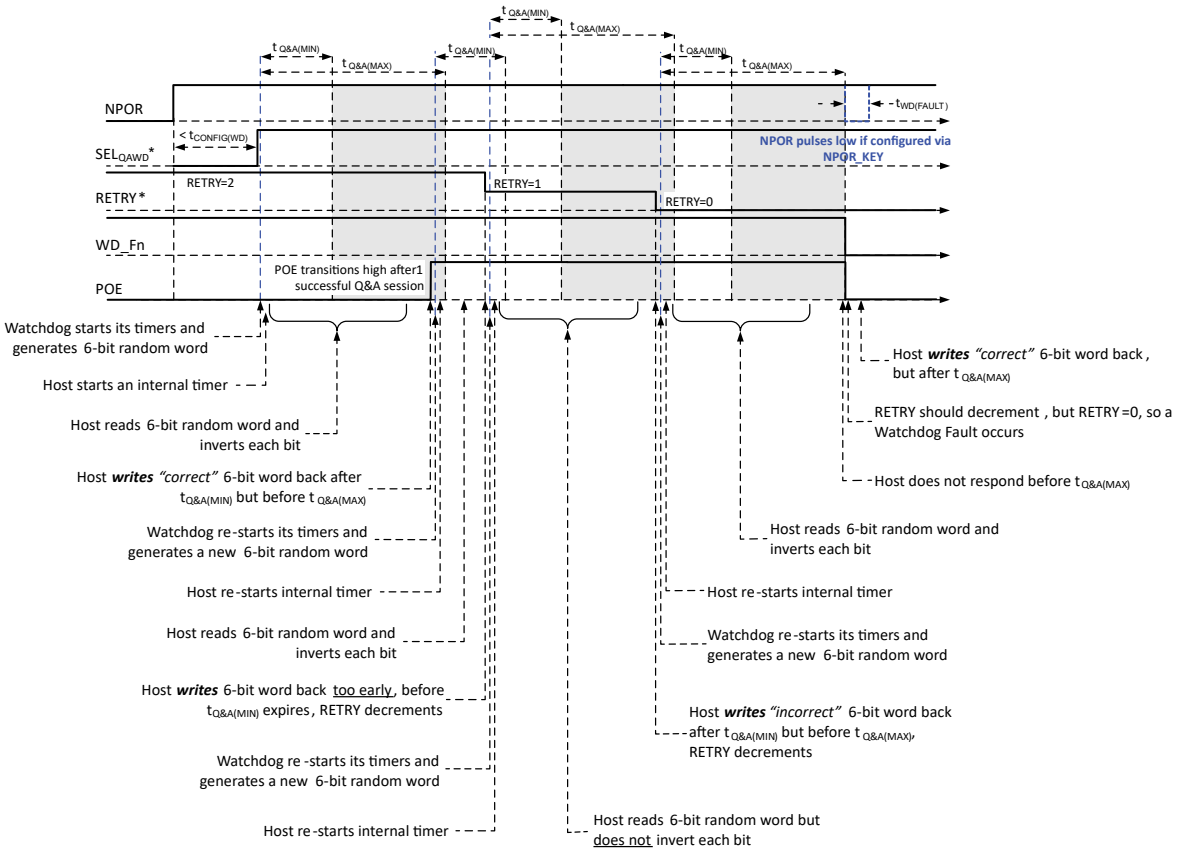

Figure 11: Q&A Selection, Operation, and Fault Examples.

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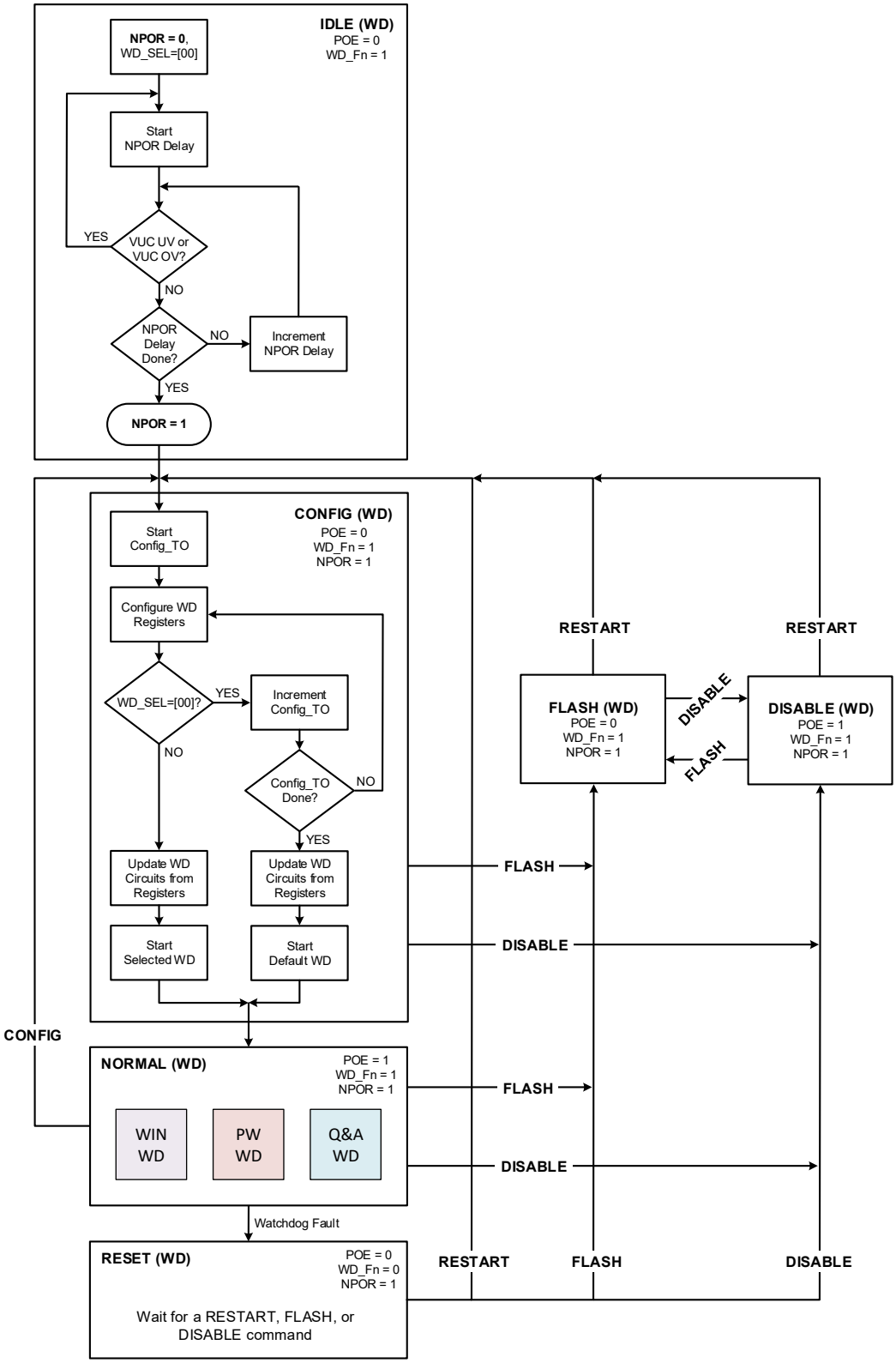

Figure 12: State Diagram of Watchdog Operation

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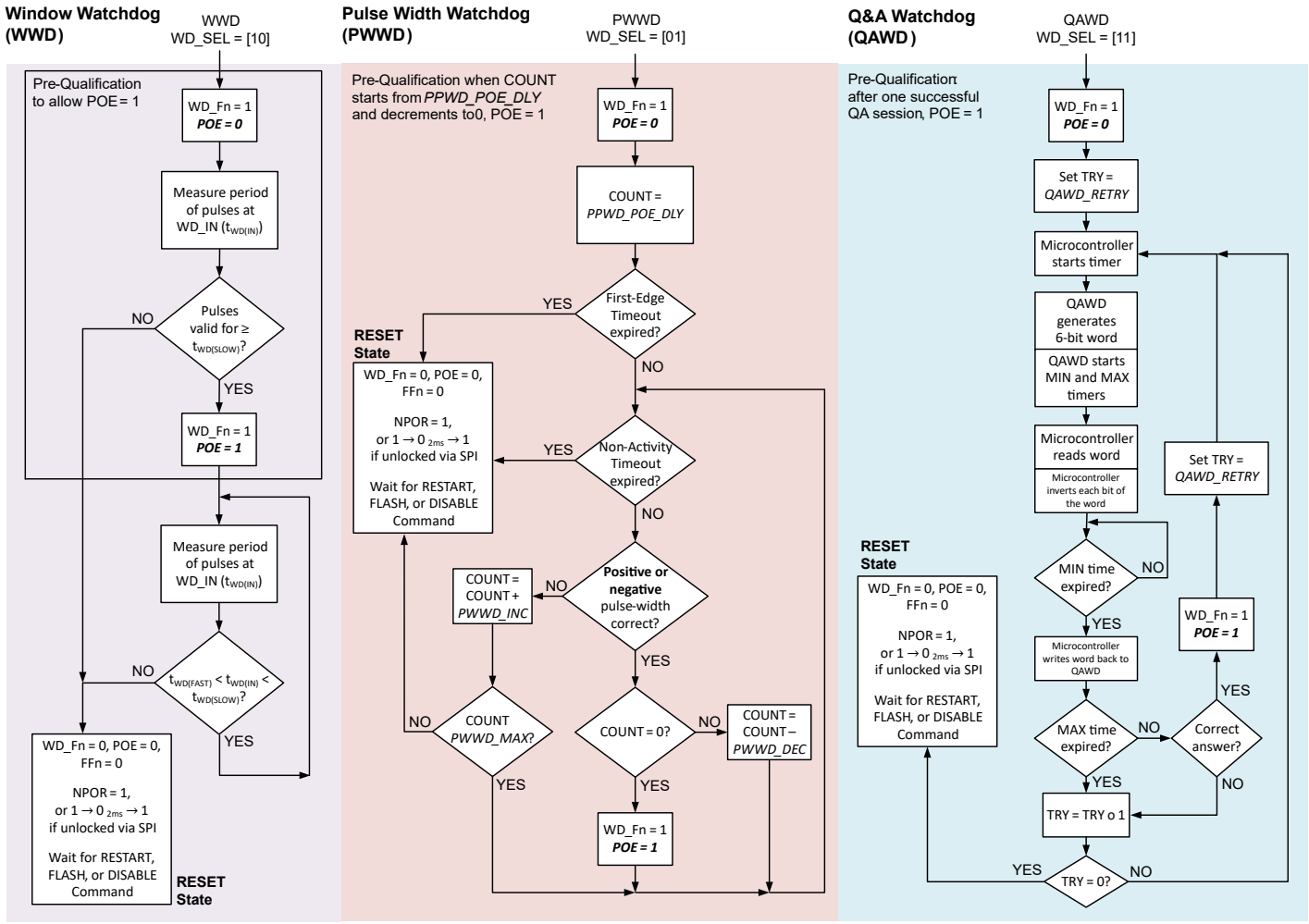

Figure 13: Watchdog Flowcharts

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SERIAL COMMUNICATION INTERFACE

The A81407 provides the user with a full-duplex, four-wire, synchronous serial interface. It is compatible with the Serial Peripheral Interface (SPI) standard using mode 3 (CPOL = 1, CPHA = 1). The SPI interface uses an "out-of-frame" communications protocol, meaning the logical response of the slave is within the next frame of the master, as shown in the following figure. The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in the Serial Interface Timing diagram (Figure 1).

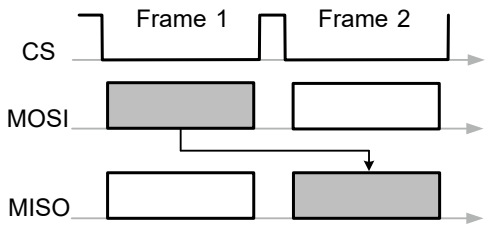

Figure 14: Out-of-Frame SPI Communication

Each 32-bit frame has a read/write bit, WR (bit 29). This bit must be set to 1 to write the subsequent bits into the selected register. If WR is set to 0 (a read), then the data bits (20 to 5) are ignored. The state of the WR bit also determines the data output on MISO. If WR is set to 1 then general diagnostic information is output. If WR is set to 0 then the contents of the register selected by the address bits is output.

MOSI: Master Output Slave Input (data input from the master). A 32-bit word, sent/received MSB first. When CS is low, data from the master is received on this pin. The slave reads/latches the data on the rising edge of SCK. The master advances to the next bit on the falling edge of SCK.

MISO: Master Input Slave Output (data output from the slave, or A81407). A 32-bit word, sent/received MSB first. This pin is high impedance when CS is high or when the Chip_ID (bit 30 from the previous frame) was incorrect. When CS is low, data from the slave is sent on this pin. The master reads/latches the data on the rising edge of SCK. The slave advances to the next bit on the falling edge of SCK.

SCK: Serial Clock (input) from the master. There must be 32 rising clock edges per frame. During each clock cycle, a full duplex data transmission occurs. The master sends a bit on the MOSI line and the slave reads it, while the slave sends a bit on the MISO line and the master reads it. This sequence is maintained even when only one-directional data transfer is intended. Data changes state on the falling edge of SCK and is latched on the rising edge of SCK. SCK must be set high before CS transitions.

CS: Chip Select (input) from the master. When CS is high MISO is high impedance, and activity on MOSI and SCK is ignored. This allows multiple SPI slaves to have common MISO, SCK, and MOSI connections. However, each slave must have a dedicated CS signal. CS is brought low to initiate a serial transfer. When 32 data bits have been clocked into the shift register, CS must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data.

If CS transitions high and there are fewer than 32 rising edges on SCK, the write will be cancelled and no data will be written to the registers. Similarly, if there are more than 32 rising edges on SCK while CS is low, the write will be cancelled and no data will be written. In both cases, the SE (serial error) and FF (Fault Flag) bits will be set high, and FFn pin (microcontroller interrupt) pulled low to indicate a data transfer error.

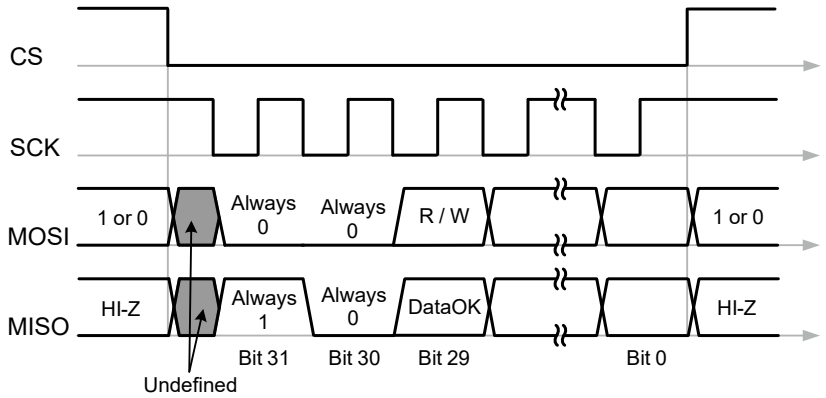

Figure 15: Example SPI Communications
Data changes on the falling edge of SCK. Data is latched on the rising edge of SCK

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SPI FRAME DEFINITIONS:

1. Chip_ID, bit 30 in both the MISO or MOSI frames, ensures that the A81407 only accepts commands meant for it when it shares SPI with a second device. For the A81407, the Chip_ID shall be internally fixed at 0. For the second device on SPI , Chip_ID should be internally fixed at 1. Seperate chip selects are still required for each device.
   An incorrect Chip_ID bit can have varying results on the MISO line. These results depend on what MISO is doing during the current frame (sending data or tri-state) and if there is an error on the MOSI data. Below table summarizes MISO response based on Chip_ID and errors.

Current Frame				Next Frame
MOSI			MISO	MISO
Bit 31	Bit 30	Error		
0	1	No	x	Tri-state
0	0	No	x	Normal response
x	x	Yes	Tri state	Tri state
x	x	Yes	Sending data	Sends error frame
1	x	No	x	Tristate

x = don't care

2. MOSI and MISO frames: include a 5-bit CRC calculated from bits 30 to bit 5.
   A. The MSB is static, so it does not need to be included in the CRC calculation. It can be checked at the Host or Device side independently.
   B. Polynomial of 0x12 ($x^5 + x^2 + 1$) is used, with a start value of 11111b and a target of 00000b.
   C. Covers every single and dual bit errors.
   D. Achieves a Hamming Distance of 3.
   E. Every 4 consecutive bit error.
   F. Line stuck low/high detected.
   G. If a CRC Error occurs, the SE and FF bits are set to 1, and the FFn pin is pulled low
3. MISO frame includes a 5-bit Message ID, bits 28 to 24.
4. MISO frame includes a 3-bit Frame Counter, bits 23 to 21.
5. Writing and reading 2-bit patterns to the read-back register checks SPI integrity.

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HOST COMMANDS:

Bits 31 is static and must be set to 0.

Bit 30, the Chip_ID, is fixed at 0 for the A81407.

Bit 29 indicates a write or a read: 1 = Write, 0 = Read.

For a read command, the data bits are considered "don't care" (DC).

Write command from the Host to the MOSI pin:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	5-bit address					DC			16-bit data																5-bit CRC				

Read command from the Host to the MOSI pin:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	5-bit address					DC			16-bit data (ignored for a read command)																5-bit CRC				

Device Responses:

Bit 31 is static, fixed at 1.

Bit 30, the Chip_ID, is fixed at 0 for the A81407

Bit 29 indicates if the 16-bit data is valid:

1 = valid data, no errors detected

0 = normal response after a MOSI Write, or an error was detected (i.e. SE or CRC) so general status bits are sent

Pattern at the MISO pin after a MOSI Read where the 16-bit data is valid (i.e. no errors detected)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	5-bit Message ID (Prev_A4:0)					Frame Counter			16-bit data																5-bit CRC				

Pattern at the MISO pin after an MOSI Write, or

Pattern at the MISO pin after an MOSI Read where the 16-bits of data are not as requested (i.e. an error was detected)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	5-bit Message ID (Prev_A4:0)					Frame Counter			FF	SE	DBE	ENBAT_S	ENB_S	POE_S	WD_F	VREG_OK	VUC_OK	V5A_OK	Not Used	Not Used	V5P1_OK	V5P2_OK	TSD_F	LX_OK	5-bit CRC				

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STATUS UPDATES AND SPI PROCEDURE IF FFN→0

The SPI diagnostic status bits of the A81407 are updated at the end of each SPI frame (i.e. when CS transitions high). This is shown by the "STATUS Latched" signal in Figure 16.

If the FFn signal transitions low, the microcontroller must immediately perform a SPI Write. To avoid inadvertently changing important configuration data, the Write should be done to the readback register (0x0C). Any 16-bits of data will suffice. At the end of this Write, the SPI diagnostic status bits will be latched.

This should capture the cause of the FFn transition. The Write operation and status update are shown as Frame 1 / $WRITE_n$ in Figure 16. After the first Write, the microcontroller should perform a second write (in this case only, a read would also be acceptable). This operation is shown as Frame 2 / $WRITE_{n+1}$ in Figure 16. During Frame 2, the 16 SPI diagnostic status bits (FF, SE, DBE, ENBAT_S, ENB_S, etc.) are clocked out on the MISO pin. If the root cause of FFn is not clear from these 16 bits, then the microcontroller must read each of the four status registers (0x00 to 0x03) to search for the root cause.

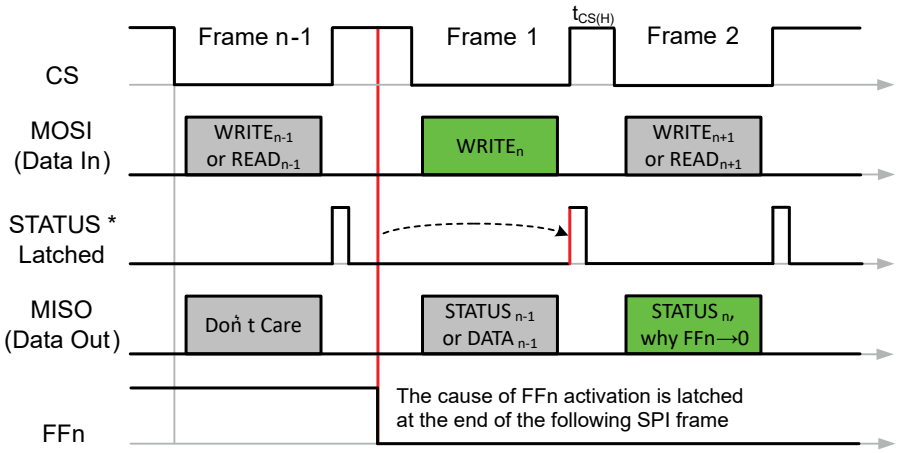

Figure 16: Recommended SPI Operations after FFn→0
* The "STATUS Latched" signal is internal to the IC

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Register Mapping

STATUS REGISTERS

The A81407 provides four status registers. These registers are read only. They provide realtime status of various functions within the A81407.

These registers report on the status of all four system rails: VUC, V5A, V5P1, and V5P2. They also report on internal rail status, such as VREG and the charge pumps. The general fault flag (FF), watchdog fault flag (WD_F), and watchdog state (WD_STATE) are found in these status registers.

CONFIGURATION REGISTERS

Four registers in the A81407 are used for configuration. Two of these registers are dedicated to setting the watchdog parameters.

The watchdog registers can only be configured while in the CONFIG state. This occurs after the A81407 is first enabled or the watchdog receives a secure SPI "RESTART" command.

The type of watchdog is selected via WD_SEL_(1:0). The default watchdog is the Pulse Width Watchdog (PWWD). The pulse width watchdog parameters are programmed in registers 0x0B.

The window watchdog (WWD) fast and slow timers are programmed in register 0x0A. The Q&A watchdog (QAWD) timers, allowed number of retries, and 6-bit random word reside in register 0x0A.

Configuration register 0x08 and 0x09 allows the user to disable the PWM dither feature, modify the response to a watchdog fault (at pins Gz and FFn), mask faults, select the battery disconnect deglitch/filter time, select the phase isolator delay time, change the safe-state of the phase isolators, and control the analog multiplexor.

ENABLE/DISABLE REGISTER

The enable/disable registers provide the user independent control of the V5Px outputs and the phase isolator gate drivers (GVBB, GU, GV, GW).

Two, nonadjacent control bits must be set to enable or disable an output. If the two bits do not match (01, or 10), then the output or gate drivers maintains its previous state.

By default, V5P1, and V5P2 are "on", but can be disabled via SPI. If either LDO is disabled its output will decay to 0 V. Normally, this would cause an UV fault to occur. However the fault flag (both FF and FFn) will not register a fault as this condition is expected and internally "masked". Both the UV and OV faults are masked when any LDO is disabled. This allows the system to disable one of the V5P LDOs and still maintain interrupt functionality to the microcontroller via the fault flag (FFn) pin. Also, if an LDO is disabled/off, the corresponding SPI diagnostic status bits (V5P1_OK or V5P2_OK) will indicate "OK", (i.e. be 1b).

Control Bits		Status Bits		FF Bit	FFn Pin
V5Px_EN_1	V5Px_EN_0	V5Px_UV	V5Px_OV		
0	0	Don't care	Don't care	Mask UV & OV	
0	1	If previous state was off		Mask UV & OV	
1	0	If previous state was off		Mask UV & OV	
1	1	1	0	1	0
1	1	0	1	1	0

WATCHDOG MODE KEY REGISTER

At times it may be necessary to reflash or restart the processor. To do this, the user should put the watchdog into "FLASH" mode. This is done by writing a sequence of keywords to the "wd_cmd_key" register. If the correct word sequence is not received, then the sequence must restart. While in FLASH mode, the A81407 sets NPOR high, WD_Fn high, and POE low.

Once flash is complete the processor must send the restart sequence of keywords for the watchdog to exit FLASH mode. If VCC has not been removed the watchdog will restart with the new configuration.

VERIFY RESULT REGISTERS

At power-up, the A81407 performs a self-test of the UV and OV detect circuits. This test should cause their diagnostic registers to toggle state. If any diagnostic register does NOT change state, the corresponding verify result register will latch high and FFn will be set low. Self-test requires much less than 1 ms at power-up, typically 350 to 500 µs.

Upon completion of power-up, the system's microcontroller may be interrupted by FFn. At that time, the microcontroller should examine the verify result registers to determine which self-test failed. If a register contains a "1", the microcontroller should make note of the failure and decide how to proceed.

Lastly, the microcontroller should write a "1" to the failed register bits (RW1C) to clear it and regain functionality of FFn.

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Table 3: Register Map

HEX Address	DEC Address	Register Name	Type	D20	D19	D18	D17	D16	D15	D14	D13
				D12	D11	D10	D9	D8	D7	D6	D5
0x00	0	status_0	RO	FF	SE	WD_Fn_S	POE_S	NPOR_S	TSD_F	DBE	UNUSED
					LX_OK	WD_Fn_OK	POE_OK	NPOR_OK		ENB_S	ENBAT_S
0x01	1	status_1	RO	VREG_OK	VUC_OK	V5A_OK			V5P1_OK	V5P2_OK	
				UNUSED	UNUSED	LG_OK	D1_OK [1]	VCP2_OK [1]		VCP_OK	
0x02	2	status_2	*RW1C, RO	*SVBB_UV	GSVBB_UV	GSU_UV	GSV_UV	GSW_UV	NPOR_IN_(1:0)		
				UNUSED	GSVBB_OV	GSU_OV	GSV_OV	GSW_OV	WD_STATE_(2:0)		
0x03	3	status_3	RO	PWWD_COUNT_(7:0)							
				UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
0x04	4	diagnostic_0	RW1C					VREG_OV	VREG_UV	VUC_OV	VUC_UV
				UNUSED	VCP_UV	V5A_OV	V5A_UV				
0x05	5	diagnostic_1	RW1C	VCP2_OV (1)	VCP2_UV (1)	UNUSED	UNUSED	V5P1_OV	V5P1_UV	V5P2_OV	V5P2_UV
				UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
0x06	6	enable/disable	RW	ENW_1	ENV_1	ENU_1	ENVBB_1	ENW_0	ENV_0	ENU_0	ENVBB_0
				V5P2_EN_1	V5P1_EN_1			V5P2_EN_0	V5P1_EN_0		
0x07	7	wd_cmd_keys	WO	WD_KEY_7	WD_KEY_6	WD_KEY_5	WD_KEY_4	WD_KEY_3	WD_KEY_2	WD_KEY_1	WD_KEY_0
		npor_inputs_key		NPOR_KEY_7	NPOR_KEY_6	NPOR_KEY_5	NPOR_KEY_4	NPOR_KEY_3	NPOR_KEY_2	NPOR_KEY_1	NPOR_KEY_0
0x08	8	config_0	RW	DITH_DIS	UNUSED	UNUSED	UNUSED				
				WDF_2_Gz	UNUSED	WDF_2_FFn	UNUSED	MASK_(3:0)			
0x09	9	config_1	RW	WD_SEL_(1:0)		GD_FLT_ON	GD_UV_SEL	GD_EN_SEL	UNUSED	UNUSED	UNUSED
				SEL_MUX_(3:0)				UNUSED	UNUSED	UNUSED	UNUSED
0x0A	10	config_2: WD [2]	RW	WWD_TIMER_(2:0)			UNUSED	QAWD_TIMER_(3:0)			
				QAWD_RETRY_(1:0)		QAWD_RAND_(5:0)					
0x0B	11	config_3: WD [2]	RW	PWWD_EDGE_TO_(1:0)		PWWD_ACT_TO_(1:0)		PWWD_WIN_TOL_(1:0)		PWWD_PW_(1:0)	
				PWWD_DEC_(1:0)		PWWD_INC_(1:0)		PWWD_MAX_(1:0)		PWWD_POE_DLY_(1:0)	
0x0C	12	readback	RW	READBACK_(15:8)							
				READBACK_(7:0)							
0x0D	13	verify_result_0	RW1C	VUC_OV_FAIL	VUC_UV_FAIL	V5A_OV_FAIL	V5A_UV_FAIL				
				BIST_FAIL	TSD_BIST_FAIL	VREG_OV_FAIL	VREG_UV_FAIL	V5P1_OV_FAIL	V5P1_UV_FAIL	V5P2_OV_FAIL	V5P2_UV_FAIL
0x0E	14	verify_result_1	RW1C			UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
				UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED

[1] Applies only if the block diagram includes this pin or function. If the pin or function does not exist the status bit will always indicate a non-fault or OK condition.
[2] With the exception of QAWD_RAND, the WatchDog (WD) registers only take effect after the state machine exits the CONFIG mode.

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0x00. Status Register 0:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	FF	SE	WD_Fn_S	POE_S	NPOR_S	TSD_F	DBE	UNUSED
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	UNUSED	LX_OK	WD_Fn_OK	POE_OK	NPOR_OK	UNUSED	ENB_S	ENBAT_S

ADDRESS: 00000b, **TYPE:** Read Only (RO)

FF [D20]	**Fault Flag**
0	No Fault (default)
1	Fault detected
SE [D19]	**Serial Communications Error**
0	No error (default)
1	Fault: less than or more than 32 rising SCK edges in a frame, or CRC Error
WD_Fn_S [D18]	**Watchdog Fault, Pin Status**
0	Fault
1	No fault or watchdog is disabled (default)
POE_S [D17]	**Power On Enable internal logic status**
0	POE is low (default)
1	POE is high
NPOR_S [D16]	**Power On Reset internal logic status**
0	NPOR is low (default)
1	NPOR is high
TSD_F [D15]	**Thermal Shutdown status**
0	Temperature is OK (default)
1	Overtemperature event
DBE [D14]	**EEPROM configuration/calibration error of 2 or more bits at power-up**
0	No fault (default)
1	Fault
UNUSED [D13:D12]	**Unused at this time.**
LX_OK [D11]	**Shows the switching node of the pre-regulator is OK**
0	Fault, LX is likely shorted to ground
1	No fault, LX is functioning/switching (default)
WD_Fn_OK [D10]	**WD_Fn pin matches what the A81407 is demanding (the WD_F bit)**
0	Fault
1	No fault (default)
POE_OK [D9]	**Power On Enable output pin matches what the A81407 is demanding**
0	Fault
1	No fault (default)
NPOR_OK [D8]	**NPOR output pin matches what the A81407 is demanding**
0	Fault
1	No fault (default)
UNUSED [D7]	**Unused at this time**
ENB_S [D6]	**Status of the logic enable input pin (ENB)**
0	ENB is low (default)
1	ENB is high
ENBAT_S [D5]	**Status of the high voltage enable input pin (ENBAT)**
0	ENBAT is low (default)
1	ENBAT is high

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0x01. Status Register 1:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	VREG_OK	VUC_OK	V5A_OK	UNUSED	UNUSED	V5P1_OK	V5P2_OK	UNUSED
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	UNUSED	UNUSED	LG_OK	D1_OK	VCP2_OK	UNUSED	VCP_OK	UNUSED

ADDRESS: 00001b, **TYPE:** Read Only (RO)

VREG_OK [D20]	**Shows the voltage at the pre-regulator output pin is within regulation**
0	Fault
1	No fault (default)
VUC_OK [D19]	**Shows the voltage at the VUC pin is within regulation**
0	Fault
1	No fault (default)
V5A_OK [D18]	**Shows the voltage at the V5A output is within regulation**
0	Fault
1	No fault (default)
UNUSED [D17:D16]	**Unused at this time**
V5P1_OK [D15]	**Shows the voltage at the V5P1 output is within regulation**
0	Fault
1	No fault (default), or V5P1 has been turned off
V5P2_OK [D14]	**Shows the voltage at the V5P2 output is within regulation**
0	Fault
1	No fault (default), or V5P2 has been turned off
UNUSED [D13:D11]	**Unused at this time**
LG_OK [D10]	**Indicates if the Boost drive, LG pin, matches the commanded value**
0	Fault
1	No fault, LG is either off (V_{VIN} > 8.5 V), or working correctly (default)
D1_OK [D9]	**Indicates if the Pre-Regulator Asynchronous diode is OK, or missing**
0	Fault, D1 is missing
1	No fault, D1 is OK (default)
VCP2_OK [D8]	**Shows the voltage at the VCP2 pin is within regulation**
0	Fault
1	No fault (default)
UNUSED [D7]	**Unused at this time**
VCP_OK [D6]	**Shows the voltage at the VCP pin is within regulation**
0	Fault
1	No fault (default)
UNUSED [D5]	**Unused at this time**

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0x02. Status Register 2:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	* SVBB_UV	GSVBB_UV	GSU_UV	GSV_UV	GSW_UV	NPOR_IN_1	NPOR_IN_0	UNUSED
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	UNUSED	GSVBB_OV	GSU_OV	GSV_OV	GSW_OV	WD_STATE_(2:0)		

ADDRESS: 00010b, **TYPE:** Read Only (RO)

SVBB_UV [D20]			**GND (–) to SVBB (+) under voltage status**
0			The voltage at the SVBB pin is OK (default)
1			The voltage at the SVBB pin is too low
GSVBB_UV [D19]			**Indicates the voltage from SVBB (–) to GVBB (+) is stuck low**
0			Gate-to-source voltage is OK (default)
1			Gate-to-source voltage is supposed to be high/on, but remains low
GSU_UV [D18]			**Indicates the voltage from SU (–) to GU (+) is stuck low**
0			Gate-to-source voltage is OK (default)
1			Gate-to-source voltage is supposed to be high/on, but remains low
GSV_UV [D17]			**Indicates the voltage from SV (–) to GV (+) is stuck low**
0			Gate-to-source voltage is OK (default)
1			Gate-to-source voltage is supposed to be high/on, but remains low
GSW_UV [D16]			**Indicates the voltage from SW (–) to GW (+) is stuck low**
0			Gate-to-source voltage is OK (default)
1			Gate-to-source voltage is supposed to be high/on, but remains low
NPOR_IN_1 [D15]	**NPOR_IN_0 [D14]**		**NPOR Input Control**
0	0		VUC_OK only (default)
0	1		VUC_OK and V5A_OK
1	0		VUC_OK and Watchdog Fault (WD_F)
1	1		VUC_OK and V5A_OK and Watchdog Fault (WD_F)
UNUSED [D13:D12]			**Unused at this time**
GSVBB_OV [D11]			**Indicates the voltage from SVBB (–) to GVBB (+) is stuck high**
0			Gate-to-source voltage is OK (default)
1			Gate-to-source voltage is supposed to be low/off, but remains high
GSU_OV [D10]			**Indicates the voltage from SU (–) to GU (+) is stuck high**
0			Gate-to-source voltage is OK (default)
1			Gate-to-source voltage is supposed to be low/off, but remains high
GSV_OV [D9]			**Indicates the voltage from SV (–) to GV (+) is stuck high**
0			Gate-to-source voltage is OK (default)
1			Gate-to-source voltage is supposed to be low/off, but remains high
GSW_OV [D8]			**Indicates the voltage from SW (–) to GW (+) is stuck high**
0			Gate-to-source voltage is OK (default)
1			Gate-to-source voltage is supposed to be low/off, but remains high
WD_STATE_2 [D7]	**WD_STATE_1 [D6]**	**WD_STATE_0 [D5]**	**WatchDog State**
0	0	0	IDLE
0	0	1	CONFIG
0	1	0	RESET
0	1	1	NORMAL
1	0	0	FLASH
1	0	1	DISABLED
1	1	0	Reserved / Future Use
1	1	1	Reserved / Future Use

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0x03. Status Register 3:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	PWWD_COUNT_(7:0)							
Data Bit / Name	D12	D11	D10	D9	D8	D7	D6	D5
	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED

ADDRESS: 00011b, **TYPE:** Read Only (RO)

PWWD_COUNT_ [D20:D13]	Indicates the value of the error counter of the Pulse Width Watchdog
00000000	0 (starting value)
.	.
.	.
.	.
10100000	160, default maximum value
.	.
.	.
11011100	220, alternate maximum value selectable via SPI
UNUSED [D12:D5]	**Unused at this time**

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0x04. Diagnostic Register 0:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	UNUSED	UNUSED	UNUSED	UNUSED	VREG_OV	VREG_UV	VUC_OV	VUC_UV
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	UNUSED	VCP_UV	V5A_OV	V5A_UV	UNUSED	UNUSED	UNUSED	UNUSED

ADDRESS: 00100b, **TYPE:** Read, or Write 1 to Clear (RW1C)

UNUSED [D20:D17]	**Unused at this time**
VREG_OV [D16]	**Indicates an overvoltage occurred at the buck pre-regulator output**
0	No fault (default)
1	Fault
VREG_UV [D15]	**Indicates an undervoltage occurred at the buck pre-regulator output**
0	No fault (default)
1	Fault
VUC_OV [D14]	**Indicates an overvoltage occurred at the VUC LDO output**
0	No fault (default)
1	Fault
VUC_UV [D13]	**Indicates an undervoltage occurred at the VUC LDO output**
0	No fault (default)
1	Fault
UNUSED [D12]	**Unused at this time**
VCP_UV [D11]	**Indicates an undervoltage occurred at the VCP pin**
0	No fault (default)
1	Fault
V5A_OV [D10]	**Indicates an overvoltage occurred at the V5A LDO output**
0	No fault (default)
1	Fault
V5A_UV [D9]	**Indicates an undervoltage occurred at the V5A LDO output**
0	No fault (default)
1	Fault
UNUSED [D8:D5]	**Unused at this time**

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0x05. Diagnostic Register 1:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	VCP2_OV	VCP2_UV	UNUSED	UNUSED	V5P1_OV	V5P1_UV	V5P2_OV	V5P2_UV
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED

ADDRESS: 00101b, **TYPE:** Read, or Write 1 to Clear (RW1C)

VCP2_OV [D20]	**Indicates an overvoltage occurred at the VCP2 pin**
0	No fault (default)
1	Fault
VCP2_UV [D19]	**Indicates an undervoltage occurred at the VCP2 pin**
0	No fault (default)
1	Fault
UNUSED [D18:D17]	**Unused at this time.**
V5P1_OV [D16]	**Indicates an overvoltage occurred at the V5P1 LDO output**
0	No fault (default)
1	Fault
V5P1_UV [D15]	**Indicates an undervoltage occurred at the V5P1 LDO output**
0	No fault (default)
1	Fault
V5P2_OV [D14]	**Indicates an overvoltage occurred at the V5P2 LDO output**
0	No fault (default)
1	Fault
V5P2_UV [D13]	**Indicates an undervoltage occurred at the V5P2 LDO output**
0	No fault (default)
1	Fault
UNUSED [D12:D5]	**Unused at this time.**

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0x06. Enable/Disable Register:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	ENW_1	ENV_1	ENU_1	ENVBB_1	ENW_0	ENV_0	ENU_0	ENVBB_0
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	V5P2_EN_1	V5P1_EN_1	UNUSED	UNUSED	V5P2_EN_0	V5P1_EN_0	UNUSED	UNUSED

ADDRESS: 00110b, **TYPE:** Read or Write (RW)

ENW_1 [D20]	**ENW_0 [D16]**	**Controls the on/off status of the GW gate driver**
0	0	Disabled (default)
0	1	Maintain previous state
1	0	Maintain previous state
1	1	Enabled
ENV_1 [D19]	**ENV_0 [D15]**	**Controls the on/off status of the GV gate driver**
0	0	Disabled (default)
0	1	Maintain previous state
1	0	Maintain previous state
1	1	Enabled
ENU_1 [D18]	**ENU_0 [D14]**	**Controls the on/off status of the GU gate driver**
0	0	Disabled (default)
0	1	Maintain previous state
1	0	Maintain previous state
1	1	Enabled
ENVBB_1 [D17]	**ENVBB_0 [D13]**	**Controls the on/off status of the GVBB gate driver**
0	0	Disabled (default)
0	1	Maintain previous state
1	0	Maintain previous state
1	1	Enabled
V5P2_EN_1 [D12]	**V5P2_EN_1 [D8]**	**Controls the on/off status of the V5P2 LDO output**
0	0	Disabled
0	1	Maintain previous state
1	0	Maintain previous state
1	1	Enabled (default)
V5P1_EN_1 [D11]	**V5P1_EN_1 [D7]**	**Controls the on/off status of the V5P1 LDO output**
0	0	Disabled
0	1	Maintain previous state
1	0	Maintain previous state
1	1	Enabled (default)
UNUSED [D10:D9]		**Unused at this time**
UNUSED [D6:D5]		**Unused at this time**

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0x07. Watchdog Command & NPOR Input Keys:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	WD_ KEY_7	WD_ KEY_6	WD_ KEY_5	WD_ KEY_4	WD_ KEY_3	WD_ KEY_2	WD_ KEY_1	WD_ KEY_0
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	NPOR_ KEY_7	NPOR_ KEY_6	NPOR_ KEY_5	NPOR_ KEY_4	NPOR_ KEY_3	NPOR_ KEY_2	NPOR_ KEY_1	NPOR_ KEY_0

ADDRESS: 00111b, **TYPE:** Write Only (WO)

WD_KEY [D20:D13]	**Watchdog Mode Key –** Three 8-bit words (WORD1 – WORD3) must be sent in the correct order to enable flash mode or restart the watchdog. If an incorrect word is receive then the register resets and the first word must be resent. The third 8-bit word (WORD3) is the command to force the Watchdog to transition from state to state.

	FLASH Command	CONFIG Command	RESTART Command	DISABLE Command
WORD1 (Key)	0xD3	0xD3	0xD3	0xD3
WORD2 (Key)	0x33	0x33	0x33	0x33
WORD3 (Command)	0xCC	0xCD	0xCE	0xCF

NPOR_KEY [D12:D5]	**NPOR Key** – Two 8-bit words (WORD1, WORD2) must be sent in the correct order to unlock the NPOR configuration register. If an incorrect word is received then the register resets and the first word must be resent. A third 8-bit word (WORD3) adds V5A_OK to the NPOR logic. If the A81407 experiences a master reset (MPOR) it will transition back to the default state.

		Inputs to the NPOR logic are		
		VUC_OK	**WD_F**	**V5A_OK**
WORD1 (Key)	0xD4	Yes (default)	No (default)	No (default)
WORD2 (Key)	0x2B			
WORD3 (Command)	0xA5	Yes	Yes (low for 2 ms)	No
	0xA6	Yes	No	Yes
	0xA7	Yes	Yes (low for 2 ms)	Yes

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0x08. Configuration Register 0:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	DITH_DIS	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	WDF_2_Gz	UNUSED	WDF_2_FFn	UNUSED	UNUSED	Pre-Reg Off	UNUSED	UNUSED

ADDRESS: 01000b, **TYPE:** Read or Write (RW)

DITH_DIS [D20]	**Controls the status of PWM frequency dithering**
0	Dithering is enabled (default)
1	Dithering is disabled
UNUSED [D19:D13]	**Unused at this time.**
WDF_2_Gz [D12]	**Determines if a watchdog fault affects the four gate drivers**
0	Gate drivers will not be affected if a WD_F occurs (default)
1	All <u>four</u> gate drivers (GVBB, GU, GV, GW) will be turned off if a WD_F occurs.
UNUSED [D11]	**Unused at this time.**
WDF_2_FFn [D10]	**Determines if a Watchdog Fault force FFn low**
0	FFn will *not* transition low if a Watchdog Fault occurs (default)
1	FFn *will* transition low if a Watchdog Fault occurs
UNUSED [D9:D8]	**Unused at this time.**
Pre-Reg Off [D7]	**Controls the masking of VREG_OV fault**
0	FFn *will* transition low if an overvoltage occurs on VREG (default)
1	FFn will *not* transition low if an overvoltage occurs on VREG
UNUSED [D6:D5]	**Unused at this time.**

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0x09. Configuration Register 1:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	WD_SEL_(1:0)		GD_FLT_ON	GD_UV_SEL	GD_EN_SEL	UNUSED	UNUSED	UNUSED
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	SEL_MUX_(3:0)				UNUSED	UNUSED	UNUSED	UNUSED

ADDRESS: 01001b, **TYPE:** Read or Write (RW)

WD_SEL_1 [D20]	WD_SEL_0 [D19]	TYPE OF ACTIVE WATCHDOG
0	0	None, power-up value for WD_SEL_(1:0)
0	1	Pulse Width Watchdog (PWWD) (default, after $t_{CONFIG(WD)}$)
1	0	Window Watchdog (WWD)
1	1	Q&A Watchdog (QAWD)
GD_FLT_ON [D18]		**Sets the fault-state of the three gate drivers, GU, GV, and GW, for any fault <u>other than a watchdog fault</u>.**
0		Fault-state of GU, GV, and GW is off. Inverse of the fault table.
1		GU, GV, and GW operate as shown in the fault table (default).
GD_UV_SEL [D17]		**Selects the gate driver under voltage filter/deglitch delay times**
0		Slow
1		Fast (default)
GD_EN_SEL [16]		**Selects the gate driver enable/disable delay times**
0		Slow
1		Fast (default)

SEL_MUX_3 [D12]	SEL_MUX_2 [D11]	SEL_MUX_1 [D10]	SEL_MUX_0 [D9]	MUX OUTPUT	DIVIDER RATIO
0	0	0	0	VREG	÷2
0	0	0	1	VUC	÷2
0	0	1	0	V5A	÷2
0	0	1	1	V5P1	÷2
0	1	0	0	V5P2	÷2
0	1	0	1	ENBAT	÷8
0	1	1	0	BG1	÷1
0	1	1	1	BG2	÷1
1	0	0	0	TEMP	**
1	0	0	1	VIN	÷10
1	0	1	0	VCP2	÷12
1	0	1	1	VCP	÷12
1	1	0	0	Unused	–
1	1	0	1	Unused	–
1	1	1	0	Unused	–
1	1	1	1	Unused	–

** V_{TEMP} = 1440 mV – 3.92 mV/°C × T_J (°C)

UNUSED [D8:D5]	Unused at this time.

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0x0A. Configuration Register 1 (WD):

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	WWD_TIMER_(2:0)			UNUSED	QAWD_TIMER_(3:0)			
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	QAWD_RETRY_(1:0)		QAWD_RAND_(5:0)					

ADDRESS: 01010b, **TYPE:** Read or Write (RW)

WWD_TIMER_2 [D20]	WWD_TIMER_1 [D19]	WWD_TIMER_0 [D18]	$t_{WD(FAST)}$ (ms)	$t_{WD(SLOW)}$ (ms)
0	0	0	0.5	4
0	0	1	1	8
0	1	0	2	16
0	1	1	4 (default)	32 (default)
1	0	0	6	42
1	0	1	8	64
1	1	0	10	80
1	1	1	12.5	100

QAWD_ TIMER_3 [D16]	QAWD_ TIMER_2 [D15]	QAWD_ TIMER_1 [D14]	QAWD_ TIMER_0 [D13]	MIN_TIMEOUT $t_{Q\&A(MIN)}$ (ms)	MAX_TIMEOUT $t_{Q\&A(MAX)}$ (ms)
0	0	0	0	0.5	1
0	0	0	1	1	2
0	0	1	0	2	4
0	0	1	1	3	8
0	1	0	0	8	16
0	1	0	1	12	24
0	1	1	0	16 (default)	32 (default)
0	1	1	1	24	48
1	0	0	0	32	64
1	0	0	1	40	80
1	0	1	0	64	128
1	0	1	1	72	144
1	1	0	0	80	160
1	1	0	1	96	192
1	1	1	0	128	256
1	1	1	1	144	288

QAWD_RETRY_1 [D12]	QAWD_RETRY_0 [D11]	ACCEPTABLE NUMBER OF RETRIES
0	0	0 times
0	1	1 time (default)
1	0	3 times
1	1	7 times

QAWD_RAND [D10:D5]	**Randomly generated 6-bit word for the Q&A watchdog.** These bits must support read (Q) and write (A) from the micro-controller during NORMAL mode of operation.

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0x0B. Configuration Register 2 (WD):

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	PWWD_EDGE_TO(1:0)		PWWD_NONACT_TO_(1:0)		PWWD_WIN_TOL_(1:0)		PWWD_PW_(1:0)	
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	PWWD_DEC_(1:0)		PWWD_INC_(1:0)		PWWD_MAX_(1:0)		PWWD_POE_DLY_(1:0)	

ADDRESS: 01011b, **TYPE:** Read or Write (RW)

PWWD_EDGE_TO_1 [D20]	PWWD_EDGE_TO_0 [D19]	FIRST-EDGE TIMEOUT (ms)
0	0	2.5
0	1	5 (default)
1	0	10
1	1	15
PWWD_ACT_TO_1 [D18]	**PWWD_ACT_TO_0 [D17]**	**NON-ACTIVITY TIMEOUT (ms)**
0	0	8
0	1	16 (default)
1	0	24
1	1	32
PWWD_WIN_TOL_1 [D16]	**PWWD_WIN_TOL_0 [D15]**	**WINDOW TOLERANCE (%)**
0	0	±8
0	1	±13 (default)
1	0	±18
1	1	±23
PWWD_PW_1 [D14]	**PWWD_PW_0 [D13]**	**PULSE WIDTH (ms)**
0	0	0.5
0	1	1.0 (default)
1	0	1.5
1	1	2.0
PWWD_DEC [D12]	**PWWD_DEC [D11]**	**DECREMENT AMOUNT (counts)**
0	0	1
0	1	2 (default)
1	0	3
1	1	4
PWWD_INC [D10]	**PWWD_INC [D9]**	**INCREMENT AMOUNT (counts)**
0	0	5
0	1	10 (default)
1	0	20
1	1	30
PWWD_MAX [D8]	**PWWD_MAX [D7]**	**MAXIMUM FAULT COUNTER VALUE**
0	0	80
0	1	120
1	0	160 (default)
1	1	220
PWWD_POE_DLY [D6]	**PWWD_POE_DLY [D5]**	Value pre-loaded into the PWWD error counter. This value is used to “pre-qualify” the WDIN clock before POE is allowed to transition high.
0	0	2 (default)
0	1	4
1	0	10
1	1	16

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0x0C. Readback Register:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	Readback_(15:8)							
Data Bit / Name	D12	D11	D10	D9	D8	D7	D6	D5
	Readback_(7:0)							

ADDRESS: 01100b, **TYPE:** Read Only (RO)

Readback [15:0]	The host microcontroller can implement a loopback test with this register. The host should write a specific pattern (value) to this register, read it back, and compare the two results. The host should use at least two different write patterns to be certain there are no stuck bits.

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0x0D. Verify Result Register 0:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	VUC_OV_FAIL	VUC_UV_FAIL	V5A_OV_FAIL	V5A_UV_FAIL	UNUSED	UNUSED	UNUSED	UNUSED
Data Bit / Name	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**
	BIST_FAIL	TSD_BIST_FAIL	VREG_OV_FAIL	VREG_UV_FAIL	V5P1_OV_FAIL	V5P1_UV_FAIL	V5P2_OV_FAIL	V5P2_UV_FAIL

ADDRESS: 01101b, **TYPE:** Read, or Write 1 to Clear (RW1C)

VUC_OV_FAIL [D20]	**Indicates if the VUC overvoltage circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
VUC_UV_FAIL [D19]	**Indicates if the VUC undervoltage circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
V5A_OV_FAIL [D18]	**Indicates if the V5A overvoltage circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
V5A_UV_FAIL [D17]	**Indicates if the V5A undervoltage circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
UNUSED [D16:D13]	**Unused at this time.**
BIST_FAIL [D12]	**Indicates if the A81407 failed one or more of its self-tests**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
TSD_BIST_FAIL [D11]	**Indicates if the TSD circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
VREG_OV_FAIL [D10]	**Indicates if the VREG overvoltage circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
VREG_UV_FAIL [D9]	**Indicates if the VREG undervoltage circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
V5P1_OV_FAIL [D8]	**Indicates if the V5P1 overvoltage circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
V5P1_UV_FAIL [D7]	**Indicates if the V5P1 undervoltage circuit passed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
V5P2_OV_FAIL [D6]	**Indicates if the V5P2 overvoltage circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.
V5P2_UV_FAIL [D5]	**Indicates if the V5P2 undervoltage circuit failed its self-test**
0	Self-test passed (default value at power-up)
1	Self-test failed. FFn set low. Write “1” to clear and regain FFn functionality.

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0x0E. Verify Result Register 1:

Data Bit / Name	D20	D19	D18	D17	D16	D15	D14	D13
	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
Data Bit / Name	D12	D11	D10	D9	D8	D7	D6	D5
	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED

ADDRESS: 01110b, **TYPE:** Read, or Write 1 to Clear (RW1C)

[D20:D5]	**Unused at this time.**

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DESIGN AND COMPONENT SELECTION

The following section briefly describes the component selection procedure for the A81407. Refer to following pages for full schematic and recommended bill of materials.

Setting Up the Pre-Regulator

This section discusses the component selection for the A81407 pre-regulator. It covers the charge pump circuit, inductor, diodes, boost MOSFET, and input and output capacitors.

Charge Pump Capacitors

The charge pump circuits require four capacitors: VCP2, a 2.2 µF capacitor connected from pin VCP to VIN and 1 µF capacitor connected between pins CP2C1 and CP2C2; and VCP, a 1 µF capacitor connected from pin VCP2 to VCP and 0.22 µF capacitor connected between pins CP1 and CP2. These capacitors should be high-quality ceramic capacitors, such as an X5R or X7R, with a voltage rating of at least 16 V.

PWM Switching Frequency

The switching frequency of the A81407 is fixed at 2.2 MHz nominal. The A81407 includes a frequency foldback scheme that starts when V_{IN} is greater than 18 V. Between 18 V and 36 V, the switching frequency will foldback from 2.2 MHz typical to 1 MHz typical. The switching frequency for a given input voltage above 18 V and below 36 V is:

Equation 1:

$$f_{SW} = 3.4 - \frac{1.2}{18} \times V_{IN}$$

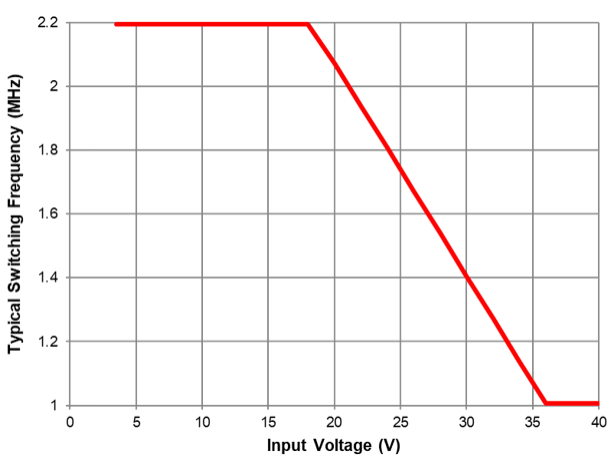

Figure 17: Typical Switching Frequency versus Input Voltage

Pre-Regulator Output Inductor

A 10 µH inductor is recommended for the pre-regulator buck and buck-boost topologies.

A molded or distributed air gap type is recommended to aid passing EMC tests. Due to topology and frequency switching of the A81407 pre-regulator, the inductor ripple current varies with input voltage per Figure 18 below.

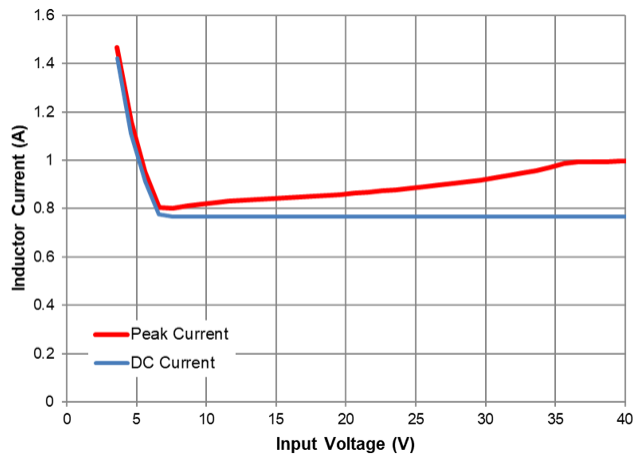

Figure 18: Typical Peak Inductor Current versus Input Voltage for 0.765 A Output Current and 10 µH Inductor

The inductor should not saturate given the peak operating current during overload. Equation 2 below calculates this current. In Equation 2, $V_{VIN(MAX)}$ is the maximum continuous input voltage, such as 16 V, and V_F is the asynchronous diode's forward voltage.

Equation 2:

$$I_{PEAK} = I_{LIM(ton,min)max} - \frac{S_E \times (V_{VREG} + V_F)}{0.9 \times f_{SW} \times (V_{VIN(MAX)} + V_F)}$$

After an inductor is chosen, it should be tested during output overload and short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure the inductor or the regulator are not damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Inductor ripple current can be calculated using equations below for buck mode, and buck-boost mode.

Equation 3:

$$\Delta I_{BUCK} = \frac{(V_{VIN} - V_{VREG}) \times V_{VREG}}{f_{SW} \times L \times V_{VIN}}$$

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Equation 4:

$$\Delta I_{BUCK} = \frac{(V_{VIN} - V_{VREG}) \times V_{VREG}}{f_{SW} \times L \times V_{VIN}}$$

Pre-Regulator Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage. They also store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{VREG}) is a function of the output capacitors parameters: C_O, ESR_{CO}, ESL_{CO}.

Equation 5:

$$\Delta V_{VREG} = \Delta I_L \times ESR_{CO} + \frac{V_{VIN} - V_{VREG}}{L} \times ESL_{CO} + \frac{\Delta I_L}{8 \times f_{SW} \times C_O}$$

The type of output capacitors will determine which terms of Equation 6 are dominant. For ceramic output capacitors, the ESR_{CO} and ESL_{CO} are virtually zero, so the output voltage ripple will be dominated by the third term of Equation 5.

Equation 6:

$$\Delta V_{VREG} = \frac{\Delta I_L}{8 \times f_{SW} \times C_O}$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply increase the total capacitance, reduce the inductor current ripple (i.e. increase the inductor value), or increase the switching frequency.

The transient response of the regulator depends on the number and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount:

Equation 7:

$$\Delta V_{VREG} = \Delta I_{LOAD} \times ESR_{CO} + \frac{di}{dt} \times ESL_{CO}$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

Ceramic Input Capacitors

The ceramic input capacitor(s) must limit the voltage ripple at the VIN pin to a relatively low voltage during maximum load. Equation 8 can be used to calculate the minimum input capacitance,

Equation 8:

$$C_{IN} \geq \frac{I_{VREG(MAX)} \times 0.25}{0.90 \times f_{SW} \times 50\ mV}$$

where $I_{VREG(MAX)}$ is the maximum current from the pre-regulator,

Equation 9:

$$I_{VREG(MAX)} = I_{LINEAR} + I_{AUX} + 20\ mA$$

where I_{LINEAR} is the sum of all the internal linear regulators output currents, I_{AUX} is any extra current drawn from the VREG output to power other devices external to the A81407.

A good design should consider the DC bias effect on a ceramic capacitor—as the applied voltage approaches the rated value, the capacitance value decreases. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature. For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size.

Also for improved noise performance, it is recommended to add smaller sized capacitors close to the input pin and the D1 anode. Use a 0.1 µF 0603 capacitor or less.

Buck-Boost Asynchronous Diode (D1)

The highest peak current in the asynchronous diode (D1) occurs during overload and is limited by the A81407. Equation 3 can be used to calculate this current.

The highest average current in the asynchronous diode occurs when V_{VIN} is at its maximum, D_{BOOST} = 0%, and D_{BUCK} = minimum (10%),

Equation 10:

$$I_{AVG} = 0.9 \times I_{VREG(MAX)}$$

where $I_{VREG(MAX)}$ is calculated using Equation 10.

Boost MOSFET (Q1)

The RMS current in the boost MOSFET (Q1) occurs when V_{VIN} is at its minimum and both the buck and boost operate at their maximum duty cycles (approximately 64% and 58%, respectively),

Equation 11:

$$I_{Q1,RMS} = \sqrt{D_{BOOST} \times \left[\left(I_{PEAK} - \frac{\Delta I_{L(B/B)}}{2}\right)^2 + \frac{\Delta I_{L(B/B)}^2}{12}\right]}$$

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where $\Delta I_{L(B/B)}$ and I_{PEAK} are derived using Equation 3 and Equation 5, respectively.

Boost Diode (D2)

In buck mode, this diode will simply conduct the output current. However, in buck-boost mode, the peak currents in this diode may increase a lot. The A81407 limits the peak current to the value calculated using Equation 3. The average current is simply the output current.

Linear Regulators

The four linear regulators only require a single ceramic capacitor located near A81407 terminals to ensure stable operation. The range of acceptable values is shown in the Electrical Characteristics table. A 2.2 µF capacitor per regulator is recommended.

Also, since the V5P1 and V5P2 are used to power remote circuitry, their load may include external wiring. The inductance of this wiring may cause LC-type ringing and negative spikes on the V5P1 (V5P2) pin if a "fast" short-to-ground occurs. A small Schottky diode is recommended to be placed close to the V5P1 (V5P2) pin to clamp this negative spike. The MSS1P5 (or equivalent) is a good choice.

Internal Bias (VCC)

The internal bias voltage should be decoupled at the VCC pin using a 1 µF ceramic capacitor. It is not recommended to use this pin as a source.

Signal Pins (NPOR, FFn, POE)

The A81407 has many signal level pins. The NPOR, FFn, and ENBAT are open-drain outputs and require external pull-up resistors. Allegro recommends sizing the external pull-up resistors so each pin will sink less than 2 mA when it is a logic low. The POE signal is push-pull output and does not require an external pull-up resistor.

Low Voltage Pins ESD Protection

Low voltage pins (ENB, CS, MOSI, SCK, MISO, AMUXO, NPOR, WD_Fn, WD_IN, FFn, and POE) are protected with a local clamp sized for ESD events as shown in Figure 19:

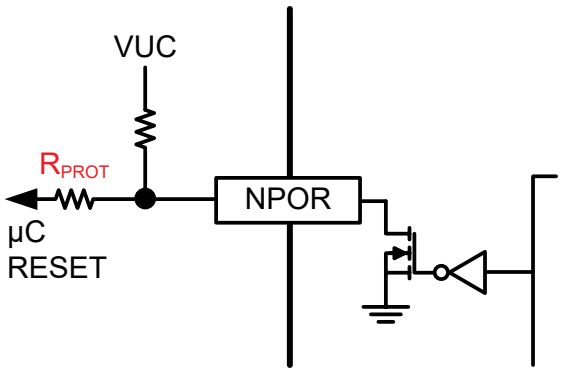

Figure 19: ESD Clamp

In case of an overvoltage condition, the ESD clamp is activated at approximately 7 V, and it is damaged unless external protection is used to limit the current, such as the R_{PROT} resistor showed in Figure 19. The R_{PROT} resistor must be sized to limit the current injected inside the pin to a maximum of 5 mA.

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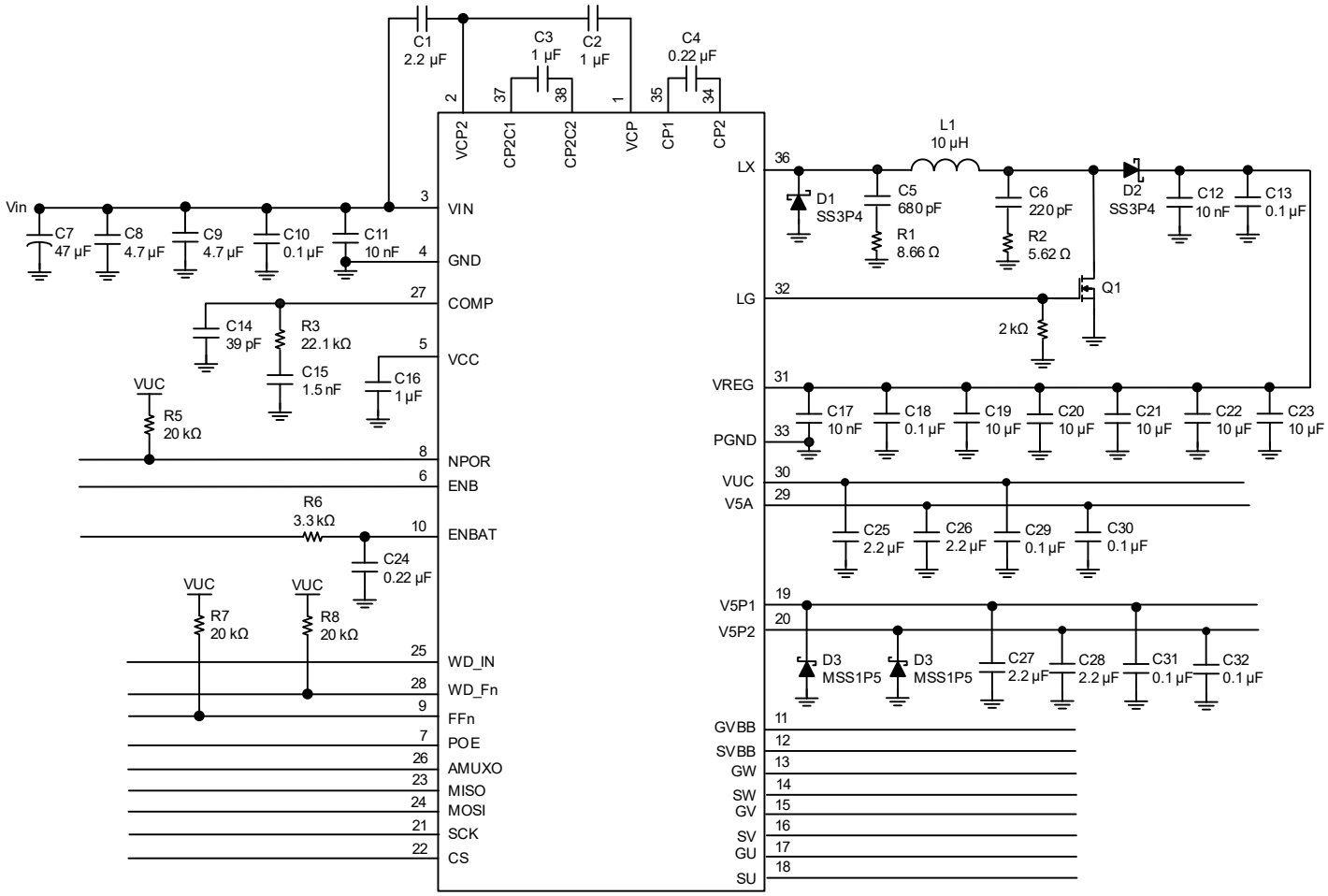

Figure 20: Typical Application Schematic

Table 4: Bill of Materials

Ref. Des.	Description	Qty.	Footprint	Manufacturer	Manufacturer P/N
U1	A81407 Buck-Boost w/ 4 LDOs, 4 Drivers, SPI	1	TSSOP-38	Allegro MicroSystems	
Q1	FET, N, 20 V / 30 V, 25 mΩ and 14 nC_{MAX} @ 4.5 V_{GS}	1	PQFN 3.3 mm × 3.3 mm	ST Onsemi Vishay	STL10N3LLH5 NVTFS4823N SQS420EN
R3	Resistor, 22.1 kΩ, 1/10 W, 1%	1	0603	Panasonic	ERJ-3EKF2212V
R5, R7, R8	Resistor, 20 kΩ, 1/10 W, 5%	3	0603	Panasonic	ERJ-3EKF2002V
R6	Resistor, 3.3 kΩ, 1/10 W, 5%	1	0603	Panasonic	ERJ-3EKF3301V
R4	Resistor, 2.00 kΩ, 1/16 W, 1%	1	0402	Vishay	CRCW04022K00FKED
R1	Resistor, 8.66 Ω, 1/4W, 1%	1	1206	Vishay	CRCW12068R66FKEA
R2	Resistor, 5.62 Ω, 1/10W, 1%	1	0603	Panasonic	ERJ-3RQF5R6V

Continued on next page...

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Table 4: Bill of Materials (continued)

Ref. Des.	Description	Qty.	Footprint	Manufacturer	Manufacturer P/N
C1	Capacitor, Ceramic, 2.2 µF, 16 V, 10%, X7R	1	0603	TDK Murata Taiyo Yuden	C1608X7S1C225K080AC GRM188Z71E225KE43D EMK107BB7225KA-T
C2, C3, C16	Capacitor, Ceramic, 1 µF, 35 V, 10%, X7R	3	0603	TDK Taiyo Yuden	C1608X7R1V105K080AC GMK107AB7105KAHT
C4, C24	Capacitor, Ceramic, 0.22 µF, 50 V, 10%, X7R	2	0603	Murata TDK	GCM188R71H224KA64J CGA3E3X7R1H224K080AB
C8, C9	Capacitor, Ceramic, 4.7 µF, 50 V, 10%, X7R	2	1210	Murata TDK Taiyo Yuden	GRM32ER71H475KA88L C3225X7R1H475K250AB UMK325B7475KM-T
C10, C13, C18, C29, C30, C31, C32	Capacitor, Ceramic, 0.1 µF, 50 V, 10%, X7R	7	0603	Murata TDK	GCM188L81H104KA57D CGA3E2X7R1H104K080AA
C19, C20, C21, C22, C23	Capacitor, Ceramic, 10 µF, 16 V, 10%, X7R	5	1206	Murata TDK Taiyo Yuden	GRM31CR71C106KAC7L C3216X7R1C106K EMK316B7106KL-TD
C25, C26	Capacitor, Ceramic, 2.2 µF, 16 V, 10%, X7R	2	0805	TDK Murata	CGA4J3X7R1C225K125AB GCM21BR71C225KA64L
C27, C28	Capacitor, Ceramic, 2.2 µF, 50 V, 10%, X7R	2	0805	TDK	CGA4J3X7R1H225M125AE
C7	Capacitor, Electrolytic, 47 µF, 35 V, 20%, 125°C	1	8mm	Nichicon Panasonic United Chemi Con	UCX1V470MCL1GS EEE-TP1V470AP EMHB350ADA470MHA0G
C14	Capacitor, Ceramic, 39 pF, 50 V, 5%, COG	1	0603	Murata TDK	GCM1885C1H390JA16D CGA2B2C0G1H390J050BA
C15	Capacitor, Ceramic, 1.5 nF, 50 V, 10%, X7R	1	0603	Murata TDK	GCM188R71H152KA37D CGA3E2X7R1H152K080AA
C11, C12, C17	Capacitor, Ceramic, 10 nF, 50 V, 10%, X7R	3	0603	TDK	CGA1A2X7R1H101K030BA
C5	Capacitor, Ceramic, 680 pF, 50 V, 10%, COG	1	0603	Murata TDK	GCM1555C1H681JA16D CGA3E2C0G1H681J080AA
C6	Capacitor, Ceramic, 220 pF, 50 V, 10%, COG	1	0603	Murata TDK	GCM1555C1H221JA16D CGA3E2C0G1H221J080AA
D1, D2	Diode, Schottky, 3 A, 40 V	2	SMP	Vishay	SS3P4-M3/84A SS3P4-M3/84A
D3, D4	Diode, Schottky, 1 A, 50 V	2	eSMP	Vishay	MSS1P5-M3/89A
L1	Inductor, 10 µH, 5.4 A_{dc}, 6.4A_{sat}, 52 mΩ max	1	8.6 mm × 8.2 mm × 4 mm	Vishay	IHLP3232DZER100M11

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PCB LAYOUT RECOMMENDATIONS

The input ceramic capacitors must be located as close as possible to the VIN pins. In general, the smaller capacitors (0402, 0603) must be placed very close to the VIN pin. The larger capacitors should be placed within 0.5 inches of the VIN pin. There must not be any vias between the input capacitors and the VIN pins.

The pre-regulator asynchronous diode (D1), input ceramic capacitors, and RC snubber must be routed on one layer and "star" grounded at a single location with multiple vias.

The pre-regulator output inductor (L1) should be located close to the LX pins. The LX trace widths (to L1, D1, and D2) should be relatively wide and preferably on the same layer as the IC.

The pre-regulators output ceramic capacitors should be located near the VREG pin. There must be 1 or 2 smaller ceramic capacitors as close as possible to the VREG pin.

The four charge pump capacitors must be placed as close as possible to VCP, CP1/CP2 and VCP2, CP2C1/CP2C2.

The ceramic capacitors for the LDOs (VUC, V5A, V5P1, and V5P2) must be placed near their output pins. The V5P1 and V5P2 outputs must have a 1 A / 40 V Schottky diode located very close to their pins to limit negative voltages.

The VCC bypass capacitor must be placed very close to the VCC pin.

The COMP network of pre-regulator (C14, C15, and R3) must be located very close to the COMP pin.

The thermal pad under the A81407 must connect to the ground plane(s) with multiple vias.

The boost MOSFET (Q1) and the boost diode (D2) must be placed very close to each other. Q1 should have thermal vias to a polygon on the bottom layer. Also, there should be "local" bypass capacitors from D2 cathode to Q1 source.

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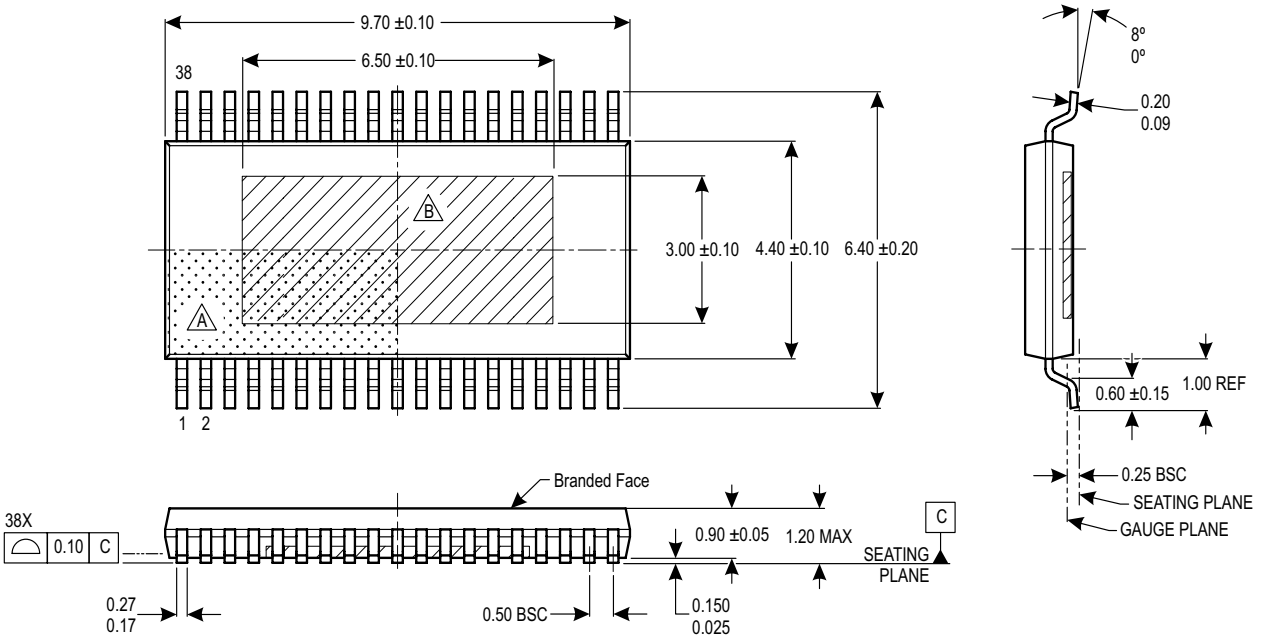
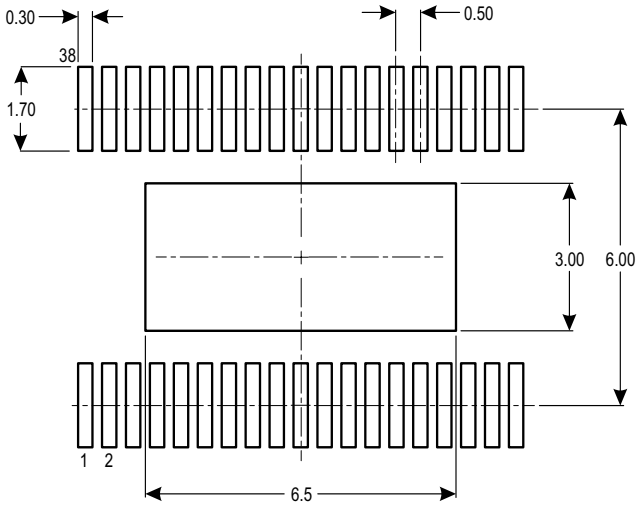
PACKAGE OUTLINE DRAWING

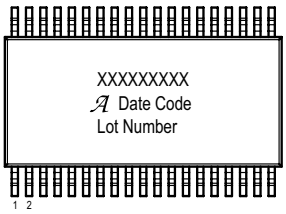
For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153 BDT-1)
Dimensions in millimeters
NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





C PCB Layout Reference View



D Standard Branding Reference View

Line 1, 2, 3 = 13 Characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP50P640X120-39M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

Figure 21: Package LV, 38-Pin eTSSOP

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Revision History

Number	Date	Description
–	December 10, 2019	Initial release
1	June 10, 2020	Updated Product Title, Features and Benefits, Description, and Applications (page 1) and Overview section (page 20).
2	December 1, 2020	Updated “CS Input Pull-Up to 3.3 V” to “CS Input Pull-Up to 3.0 V” (page 14).
3	February 1, 2021	Changed minimum values of $t_{SCK(H)}$ and $t_{SCK(L)}$ from 50 ns to 40 ns (page 14).
4	February 9, 2022	Updated package drawing (page 57).
5	November 27, 2023	Removed “(pending)” from ASIL logo (page 1); updated Functional Block Diagram (page 4).
6	February 25, 2026	Updated ASIL logo and bullet (page 1).
7	April 15, 2026	Added Low Voltage Pins ESD Protection section (page 53).

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